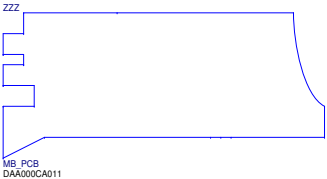


MODEL NAME : CAZ00
PCB NO : LA-D841P
BOM P/N : DAA000CA010



Dell/Compal Confidential

Schematic Document

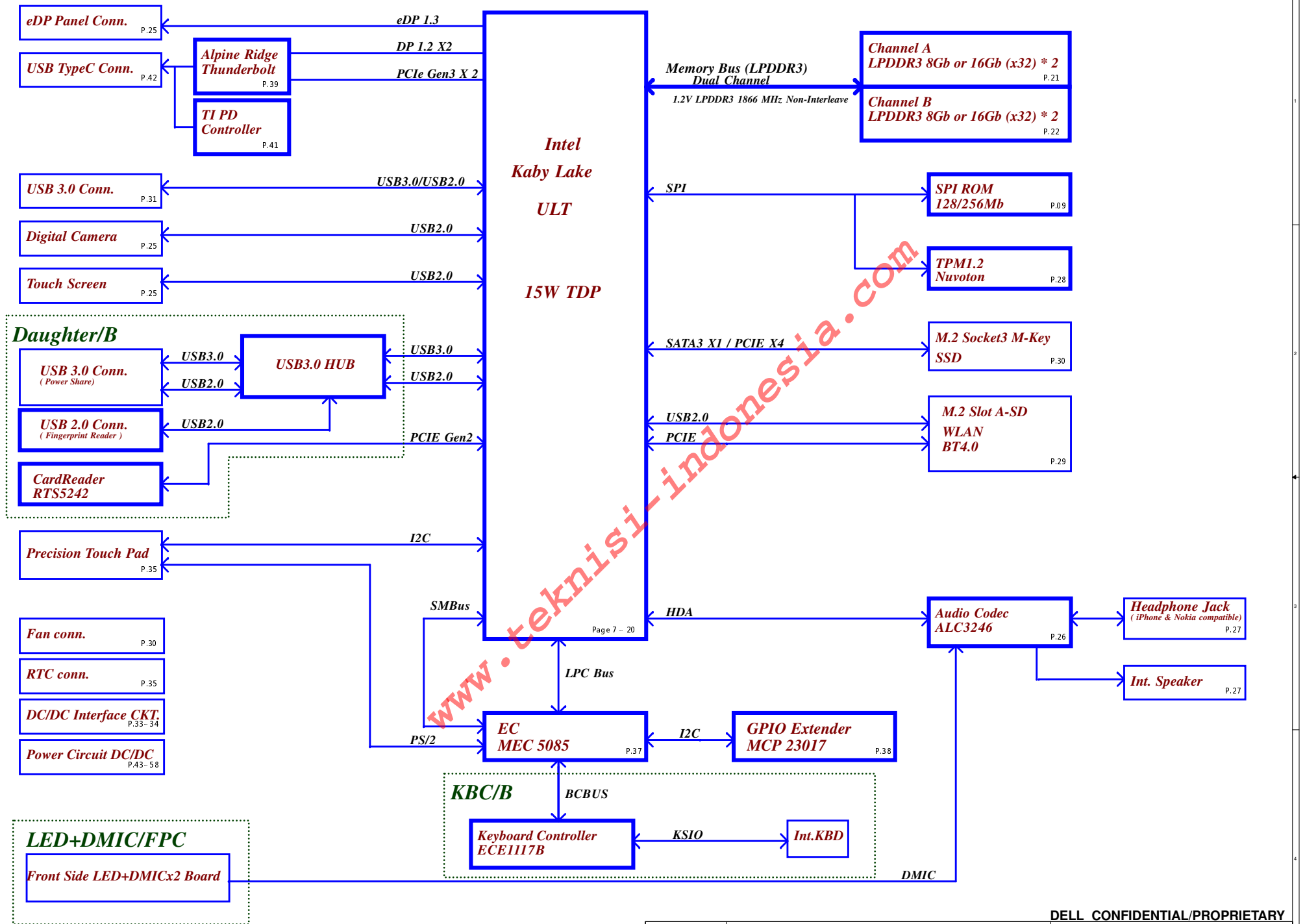
Dino2 MLK (Kaby Lake ULT)

2016-06-21

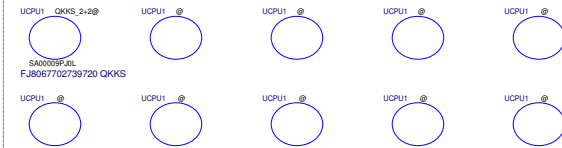
Rev: 1.0 (A00)

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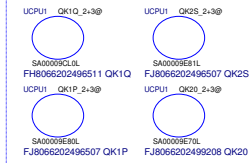
Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		Deciphered Date		Compal Electronics, Inc.	
2016/12/16		2016/12/13		Title	
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		Document Number		1.0	
		LA-D841P		Date: Wednesday, August 31, 2016	
				Sheet 1 of 60	



2+2 CPU Option



2+3 CPU Option



AR Option



DRAM Option

DRAM Config Option

	UD19 MAG 1866@	UD20 MAG 1866@	UD21 MAG 1866@	UD22 MAG 1866@	MEM_CONFIG0 RH144 MAG 1866@	MEM_CONFIG1 RH139 MAG 1866@	MEM_CONFIG2 RH145 MAG 1866@	MEM_CONFIG3 RH151 MAG 1866@	MEM_CONFIG4 RH147 MAG 1866@
Micron 4G/1866	SA00008PF1L EDF8132A3MA-JD-F-R A311	SA00008PF1L EDF8132A3MA-JD-F-R A311	SA00008PF1L EDF8132A3MA-JD-F-R A311	SA00008PF1L EDF8132A3MA-JD-F-R A311	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Micron 8G/1866	SA00008Q11L EDFA232A2MA-JD-F-R A311	SA00008Q11L EDFA232A2MA-JD-F-R A311	SA00008Q11L EDFA232A2MA-JD-F-R A311	SA00008Q11L EDFA232A2MA-JD-F-R A311	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%	SD028100280 10K_0402_5%
Hynix 4G/1866	SA00008G61L H9CCNN8GTMLAR-NUD	SA00008G61L H9CCNN8GTMLAR-NUD	SA00008G61L H9CCNN8GTMLAR-NUD	SA00008G61L H9CCNN8GTMLAR-NUD	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Hynix 8G/1866	SA00008FJ1L H9CCNN8GTMLAR-NUD	SA00008FJ1L H9CCNN8GTMLAR-NUD	SA00008FJ1L H9CCNN8GTMLAR-NUD	SA00008FJ1L H9CCNN8GTMLAR-NUD	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 4G/1866	SA00008PO1L K4EBE304EE-EGCF A311	SA00008PO1L K4EBE304EE-EGCF A311	SA00008PO1L K4EBE304EE-EGCF A311	SA00008PO1L K4EBE304EE-EGCF A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 8G/1866	SA00008QV1L K4EBE304EE-EGCF A311	SA00008QV1L K4EBE304EE-EGCF A311	SA00008QV1L K4EBE304EE-EGCF A311	SA00008QV1L K4EBE304EE-EGCF A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Micron 16G/1866	SA00008QW1L EDFB232A1MA-JD-F-R A311	SA00008QW1L EDFB232A1MA-JD-F-R A311	SA00008QW1L EDFB232A1MA-JD-F-R A311	SA00008QW1L EDFB232A1MA-JD-F-R A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 16G/2133	SA00008VV1L K4EBE304EB-EGCG A311	SA00008VV1L K4EBE304EB-EGCG A311	SA00008VV1L K4EBE304EB-EGCG A311	SA00008VV1L K4EBE304EB-EGCG A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Samsung 16G/1866	SA00008X11L K4EBE304EB-EGCF A311	SA00008X11L K4EBE304EB-EGCF A311	SA00008X11L K4EBE304EB-EGCF A311	SA00008X11L K4EBE304EB-EGCF A311	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D
Hynix 16G/1866	SA00008YT1L H9CCNN8GTMLAR-NUD	SA00008YT1L H9CCNN8GTMLAR-NUD	SA00008YT1L H9CCNN8GTMLAR-NUD	SA00008YT1L H9CCNN8GTMLAR-NUD	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D	SD028100280 10K_0402_5%-D

Board ID Table for AD channel

RE79	CE54	REV
240K	4700p	TBD
130K	4700p	TBD
62K	4700p	A00
33K	4700p	X02
8.2K	4700p	X01
4.3K	4700p	X00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%

	SKU	PTT	TPM2.0
Dino2 MLK	Vpro+CS	Disable	Enable
	nVpro+CS	Enable	None

SMBUS Control Table


	SOURCE	23017	BATTERY	Charger	PD	5085	XDP	Audio	Touch Pad
I2C1A_CLK I2C1A_DATA	MEC5085	V							
I2C1C_CLK I2C1C_DATA	MEC5085		V						
I2C1G_CLK I2C1G_DATA	MEC5085			V					
I2C2A_CLK I2C2A_DATA	MEC5085				V				
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH					V			
SMBCLK SMBDATA	PCH						V		
I2C0_CLK I2C0_DATA	PCH								
I2C1_CLK I2C1_DATA	PCH								V


CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Alpine Ridge
	CLKOUT_PCIE1	NGFF CARD WLAN	Lane 2	Alpine Ridge
	CLKOUT_PCIE2		Lane 3	
	CLKOUT_PCIE3	M.2 SSD / PCIe	Lane 4	
	CLKOUT_PCIE4		Lane 5	NGFF CARD WLAN
	CLKOUT_PCIE5	Card Reader	Lane 6	Card Reader
	FLEX CLK#	DESTINATION	Lane 7	
	CLKOUT_LPC_0	EC LPC	Lane 8	
	CLKOUT_LPC_1	Debug	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

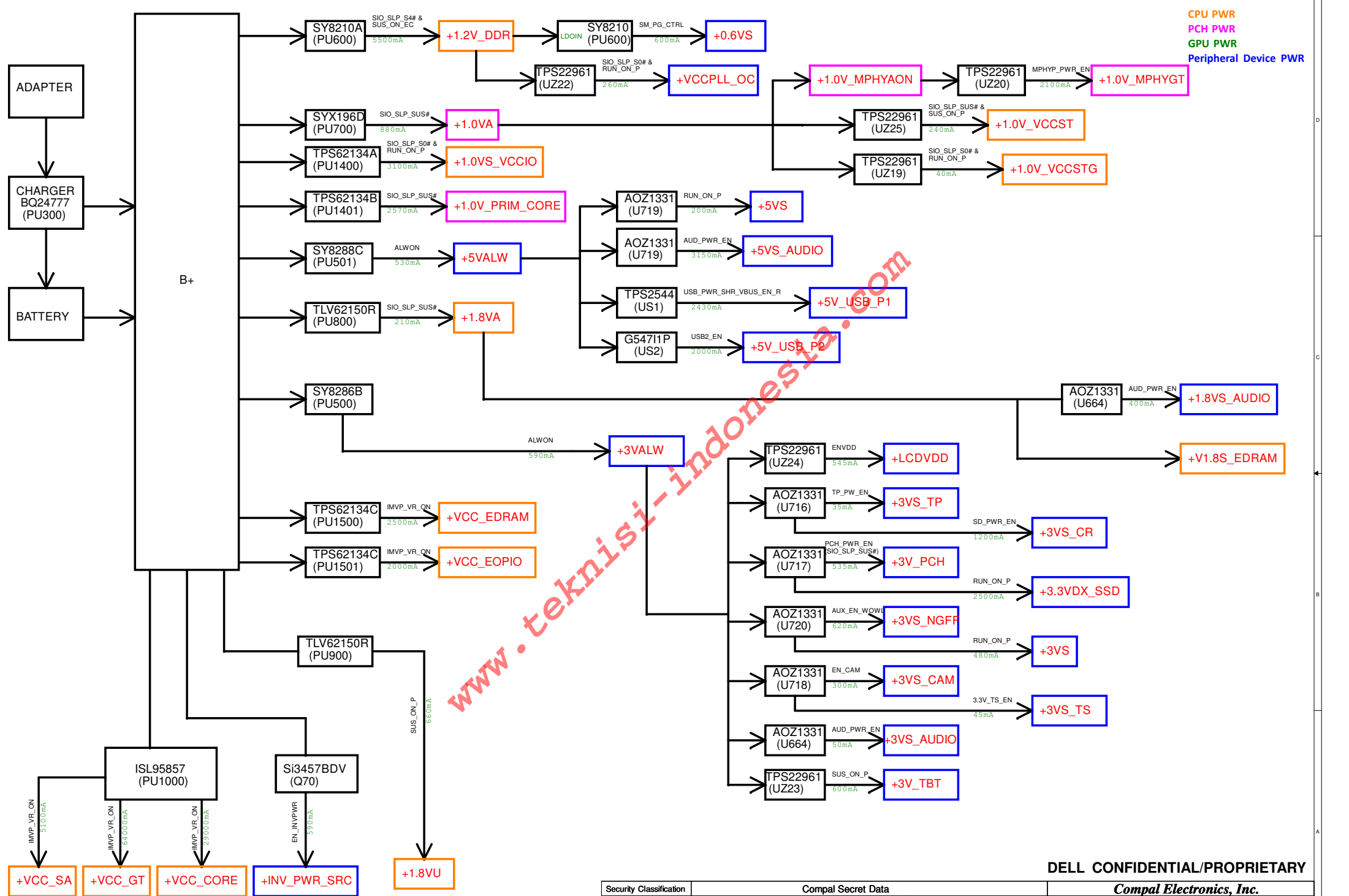
PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	External USB3(On IOB)
	2	External USB3(On MB)
	3	NGFF CARD WLAN
	4	Touch Panel
	5	Camera
	6	
	7	
PCH USB 3.0 Port Mapping	1	External USB3(On IOB)
	2	External USB3(On MB)
PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

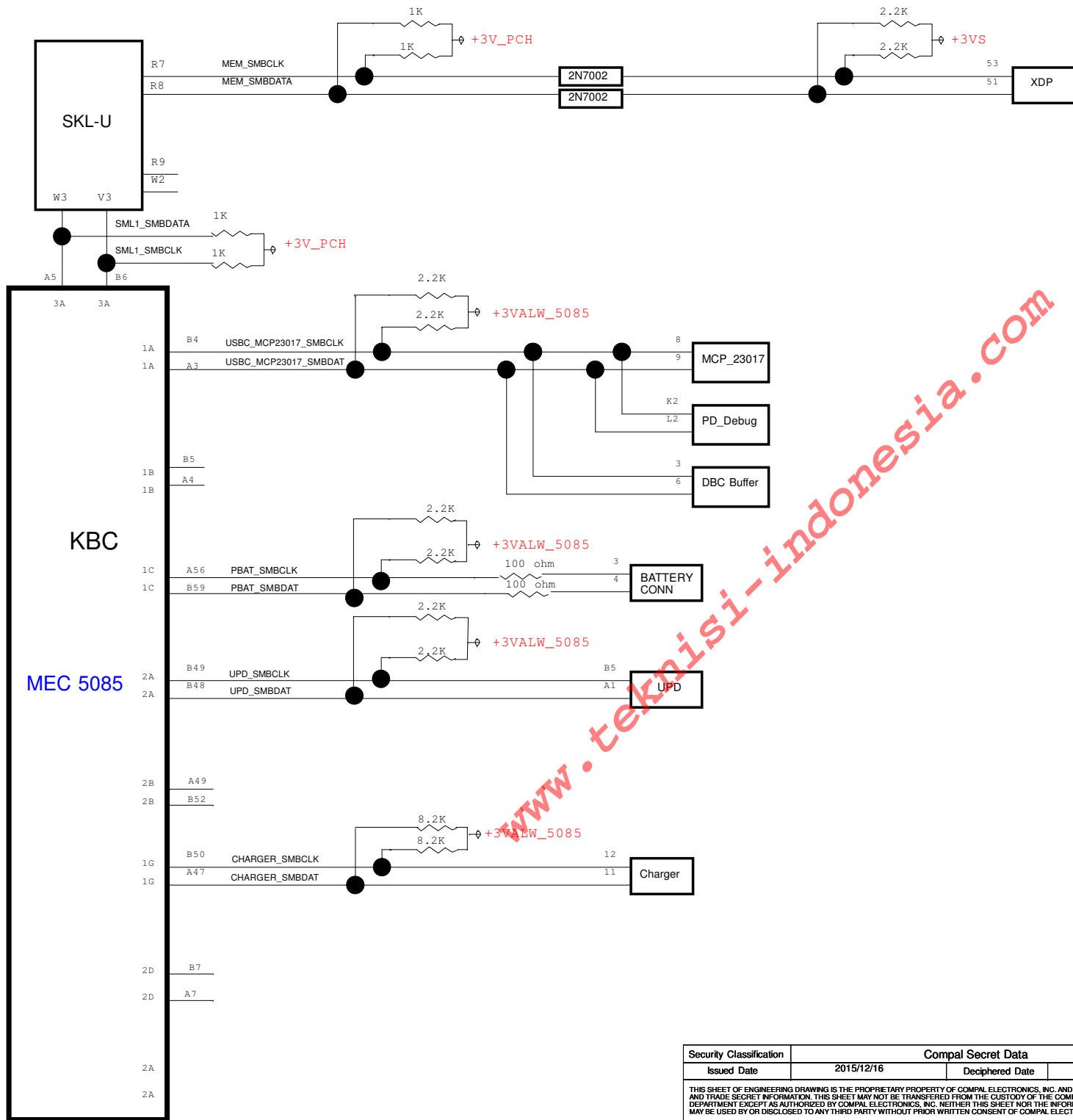
SATA PORT#	DESTINATION
SATA-0	
SATA-1A	
SATA-1B	
SATA-2	M.2 SSD

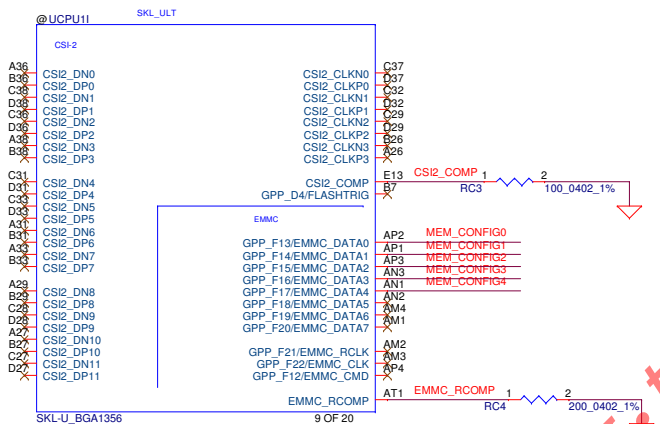
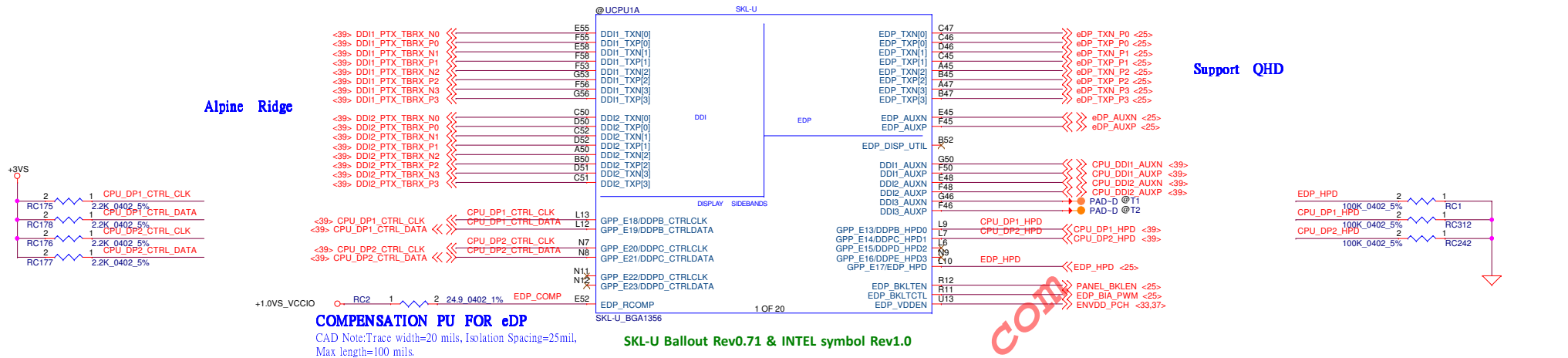
Symbol Note :

 : means Digital Ground

 : means Analog Ground





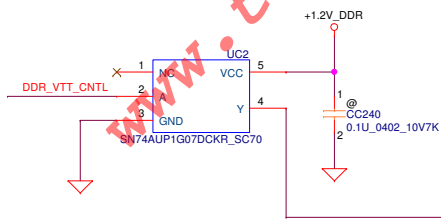
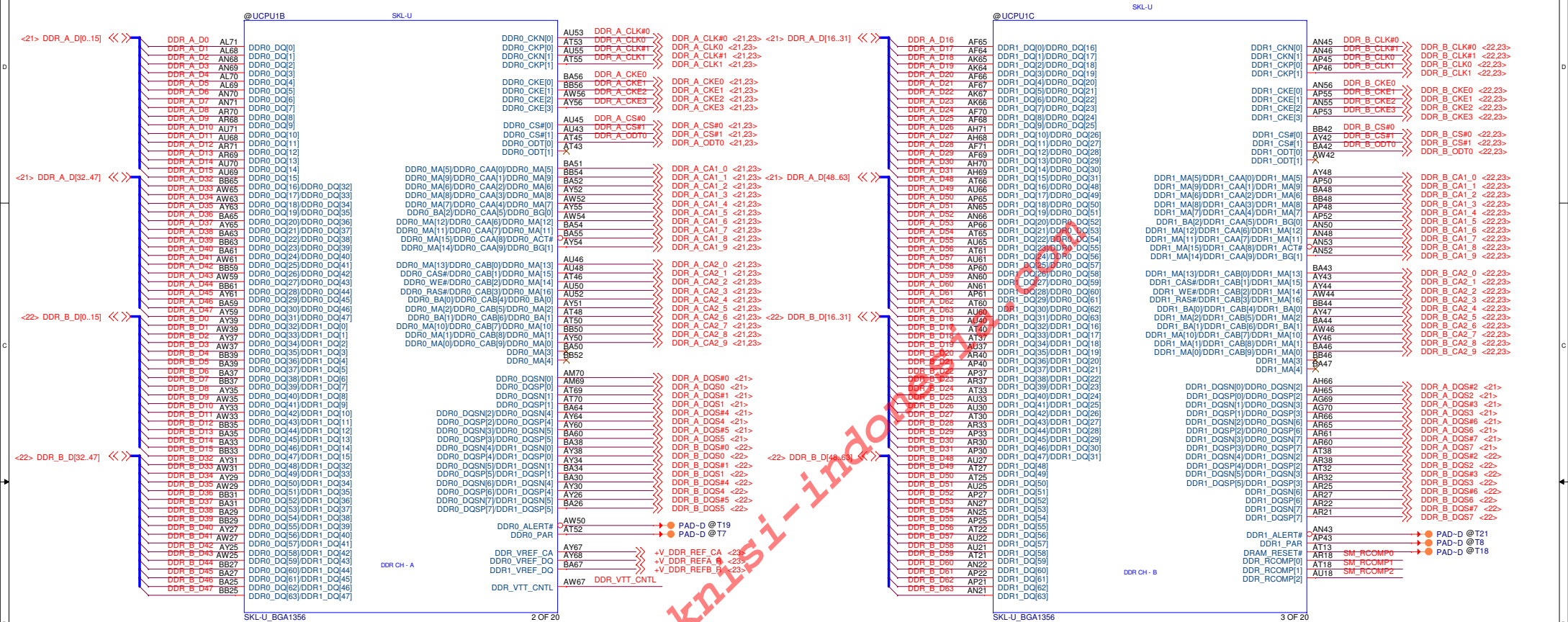


GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1	0	0	1	1	0	0	1	1	0
GPP_D7	MEM_CONFIG2	0	0	0	0	1	1	0	0	0
GPP_D8	MEM_CONFIG3	0	0	0	0	0	0	0	0	1
GPP_D9	MEM_CONFIG4	0	0	0	0	0	0	0	0	0

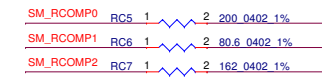
GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1	0	1	0	1	0	1	0	1
GPP_D6	MEM_CONFIG1	0	1	1	0	0	1	1	0	0
GPP_D7	MEM_CONFIG2	0	0	0	1	1	1	1	0	0
GPP_D8	MEM_CONFIG3	1	1	1	1	1	1	1	0	0
GPP_D9	MEM_CONFIG4	0	0	0	0	0	0	0	1	1

GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1	1	1	0	0	1	1	0	0	1
GPP_D7	MEM_CONFIG2	0	0	1	1	1	1	0	0	0
GPP_D8	MEM_CONFIG3	0	0	0	0	0	0	1	1	1
GPP_D9	MEM_CONFIG4	1	1	1	1	1	1	1	1	1

LPDDR3, Ballout for side by side(Non-Interleave)



LPDDR3 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

Security Classification	Compal Secret Data		
Issued Date	2015/12/16	Deciphered Date	2016/12/13
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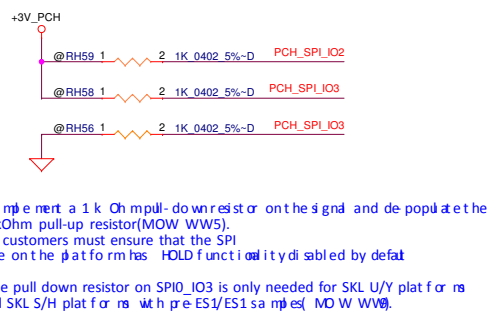
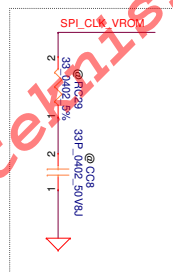
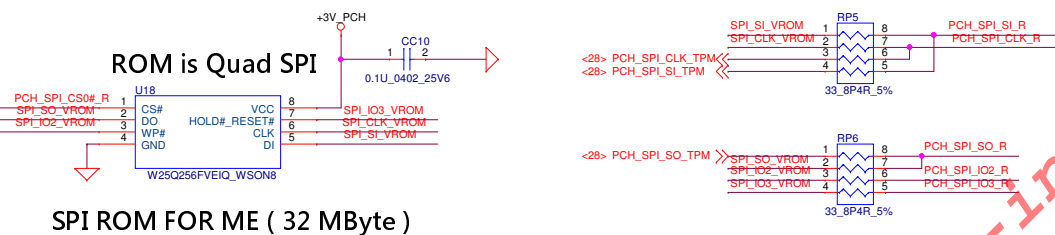
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Title	<i>P08-MCP(2/14)LPDDR3</i>
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Size	Document Number	Rev
	FA 80-15B	10

LA-D841P



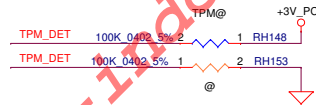
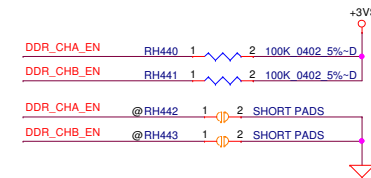
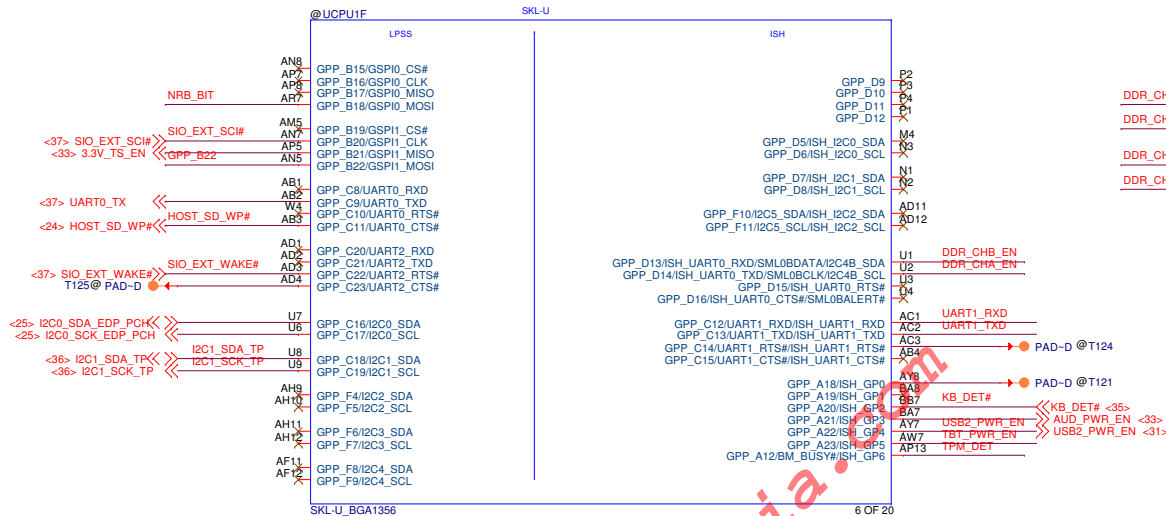
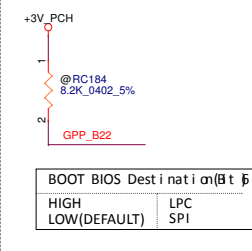
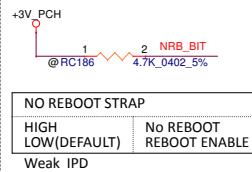
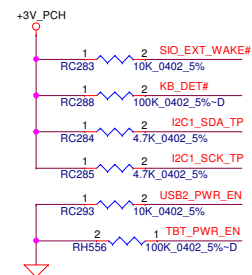
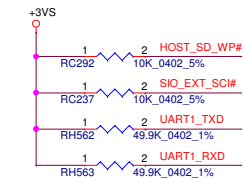
08/05: R26 BIOS set this signal to GPIO,
Refer PCH EDS reserve to 150K NC)

GPP_B23 @RC26

1 2

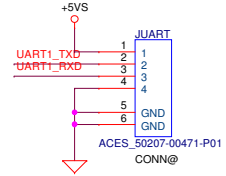
150K_0402_1%

EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE



TPM BOM Optional

TPM DET	
TPM	1 = W/TPM
	0 = W/O TPM



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Issued Date	2015/12/16	Deciphered Date	2016/12/13	P10-MCP(4/14)GSPI,I2C,UART,ISH	
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					LA-D841P
				Date:	Wednesday, August 31, 2016
				Sheet	10 of 60
				Rev	1.0

M.2 SSD
PCIe Gen3 x 4

SATA SSD

WLAN
PCIe Gen2 x 1

Cardreader
PCIe Gen2 x 1

Alpine Ridge
PCIe Gen3 x 2

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<39> PCIE_PRX_TBXTX_P1
<39> PCIE_PTX_TBRTX_N1
<39> PCIE_PTX_TBRTX_P1
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<29> PCIE_PTX_WLANRX_N5
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<30> SATA_PTX_SSDRX_P2

@UCPU1H

SKL-U

PCIe/USB3/SATA

SSC / USB3

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP
G11 PCIE2_RXN/USB3_6_RXN
E11 PCIE2_RXP/USB3_6_RXP
D19 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

H18 PCIE3_RXN
C18 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP
G15 PCIE4_RXN
B15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP
G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP
G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

E22 PCIE9_RXN
D22 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP
F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

F5 PCIE_RCOMP_N
E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

E27 PCIE11_RXN/SATA1B_RXN
D24 PCIE11_RXP/SATA1B_RXP
C24 PCIE11_TXN/SATA1B_TXN
E30 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
A25 PCIE12_RXP/SATA2_RXP
B25 PCIE12_TXN/SATA2_TXN
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E5 PCIE_RCOMP_P
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D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

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E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

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D56 PROC_PRDY#
D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

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E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

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D61 PROC_PREQ#
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D61 PROC_PREQ#
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D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

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E5 PCIE_RCOMP_P
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D61 PROC_PREQ#
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D61 PROC_PREQ#
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E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

F5 PCIE_RCOMP_N
E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
B11 GPP_A7/PIRQA#

USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP
USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP
USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP
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USB3_4_RXP
USB3_4_TXN
USB3_4_TXP

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USB3_1_RXP
USB3_1_TXN
USB3_1_TXP
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D13 USB3TP1 <24>

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USB3.0 IO/B Side

USB3.0 M/B Side

USB2.0 IO/B Side

USB2.0 M/B Side

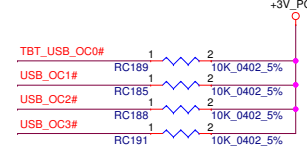
NGFF (WLAN)

Touch Panel

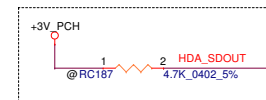
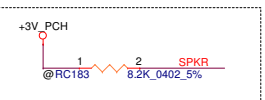
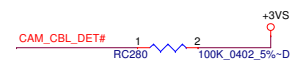
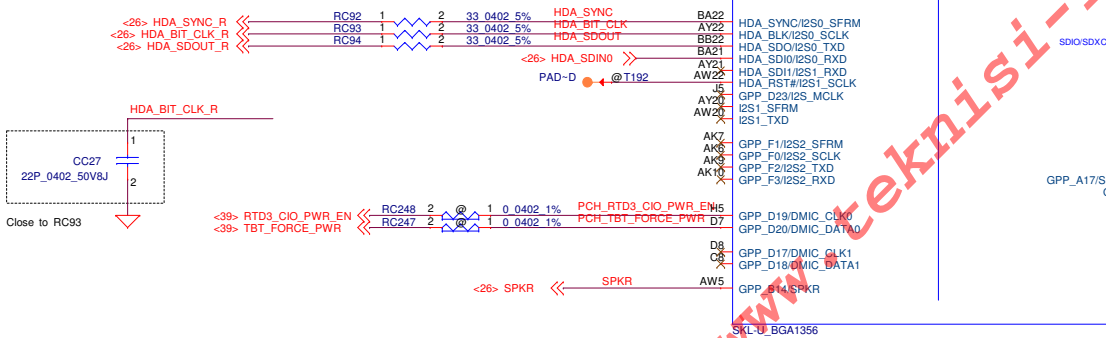
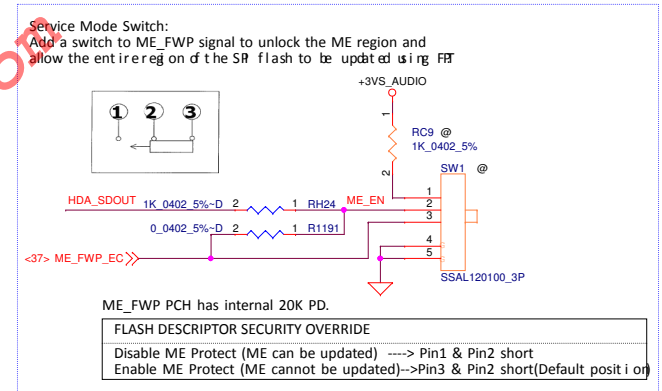
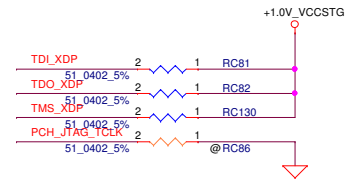
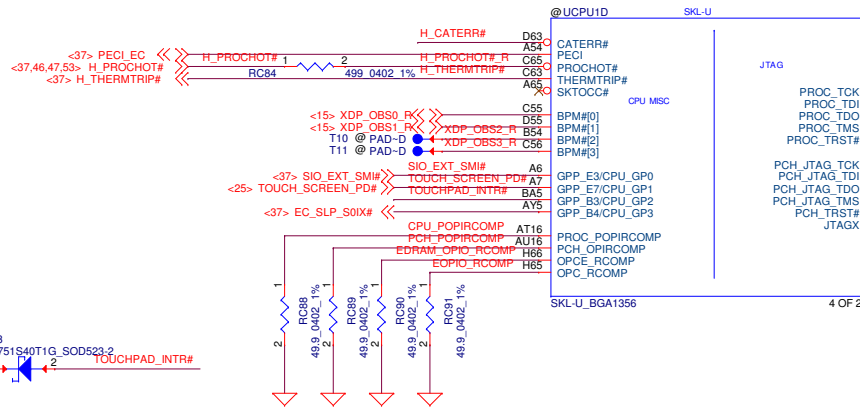
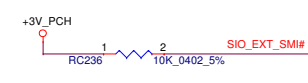
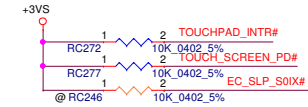
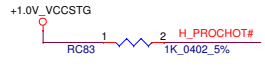
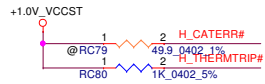
Camera

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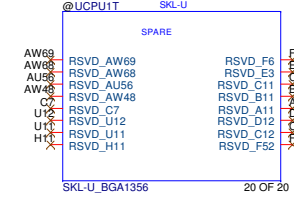
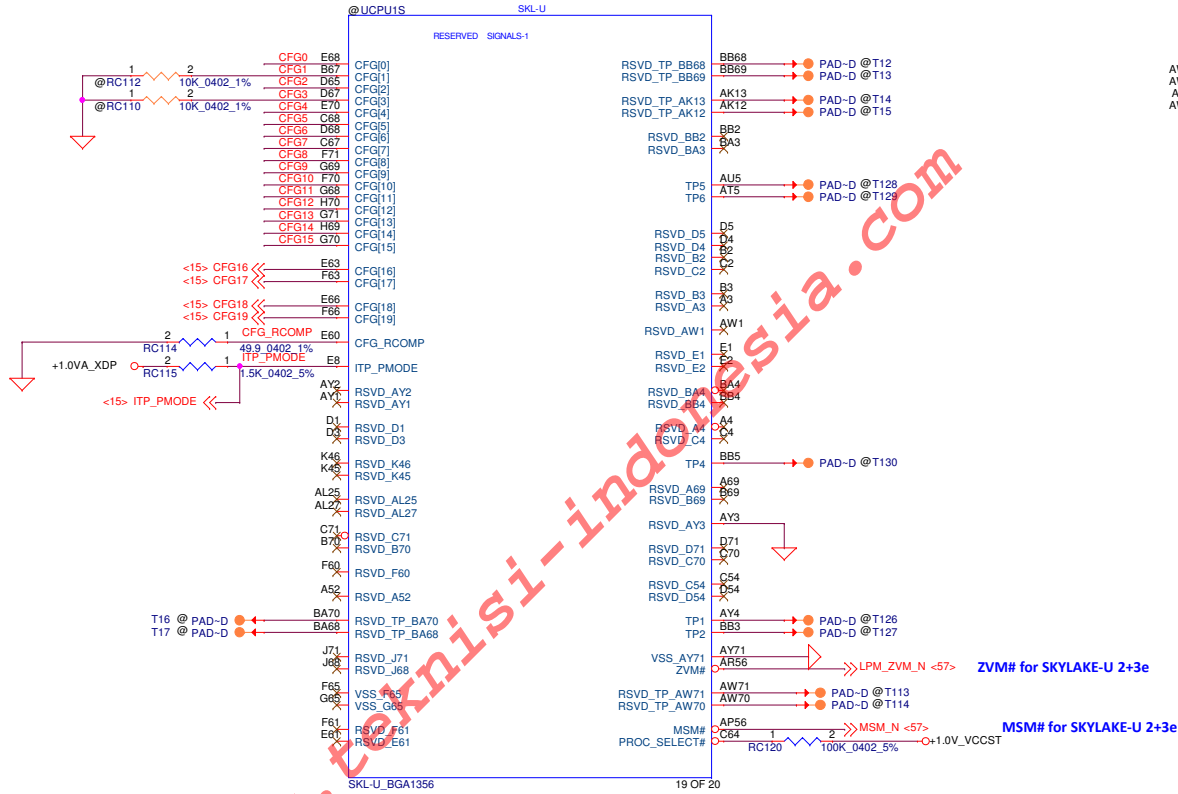
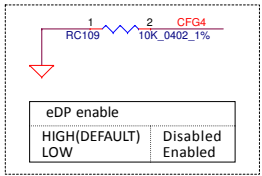
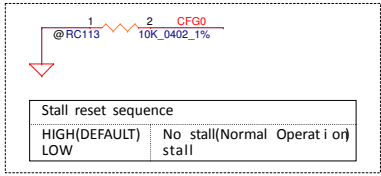
Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				2015/12/16				Compal Electronics, Inc.			
Deciphered Date				2016/12/13				P11-MCP(5/14)PCIE,USB,SATA			
Title				Document Number				LA-D841P			
Date				Wednesday, August 31, 2016				Rev 1.0			
Sheet				11				of 60			

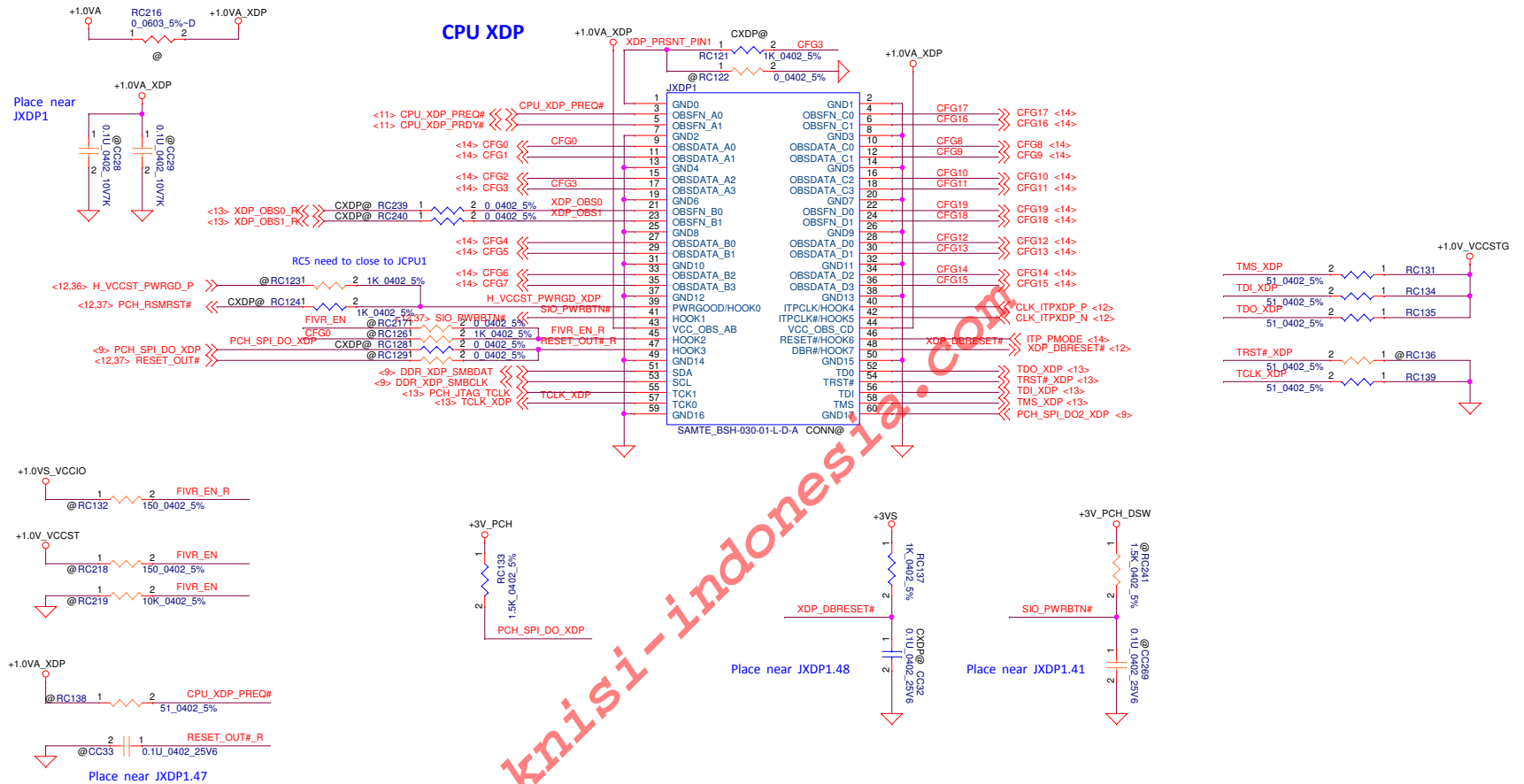


TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	P13-MCP(7/14)MISC,JTAG,HDA,SDIO
				Size	Document Number
				LA-D841P	
				Rev	1.0
				Date	Wednesday, August 31, 2016
				Sheet	13 of 60

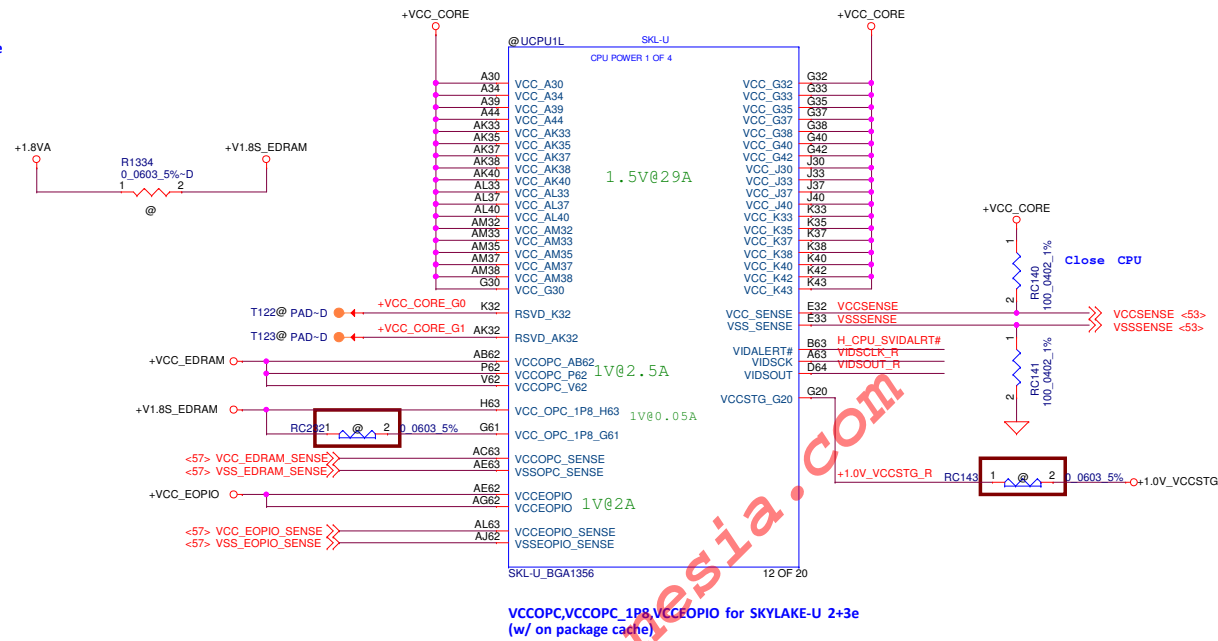




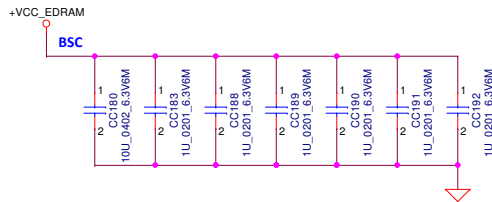
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

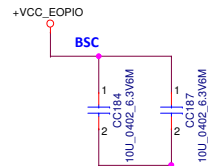
+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A



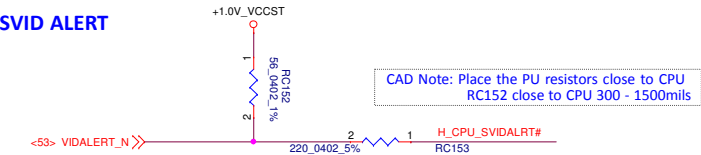
+VCC_EDRAM Decoupling Requirement
Back Side (underneath the package):
10U_0402*1 pcs + 1U_0201*6 pcs



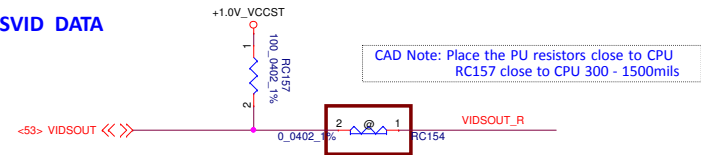
+VCC_EOPIO Decoupling Requirement
Back Side (underneath the package):
10U_0402*2 pcs



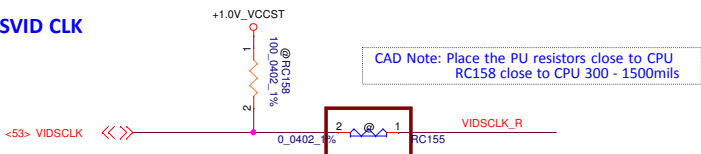
SVID ALERT



SVID DATA

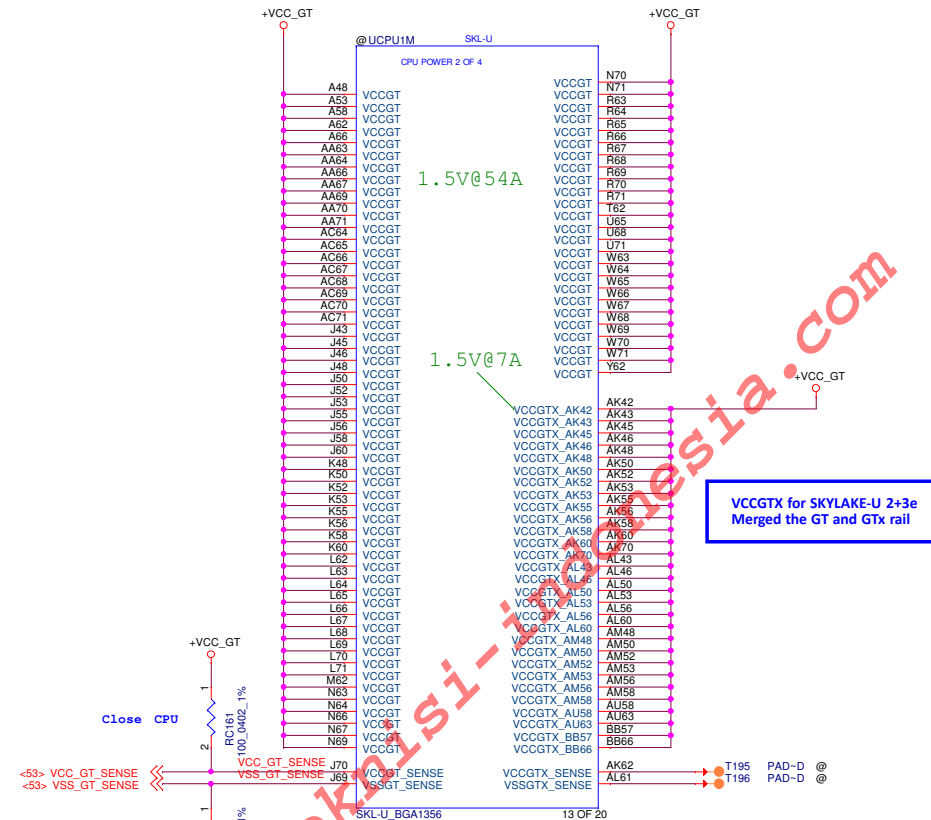


SVID CLK



Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				2015/12/16				Compal Electronics, Inc.			
Deciphered Date				2016/12/13				Title			
								P16-MCP(10/14)PWR-VCC CORE			
								Size Document Number			
								LA-D84IP			
								Rev 1.0			
								Date: Wednesday, August 31, 2016			
								Sheet 16 of 60			

+VCCGT: 0.55~1.5V, 54A
+VCCGTx : 0.55~1.5V, 7A

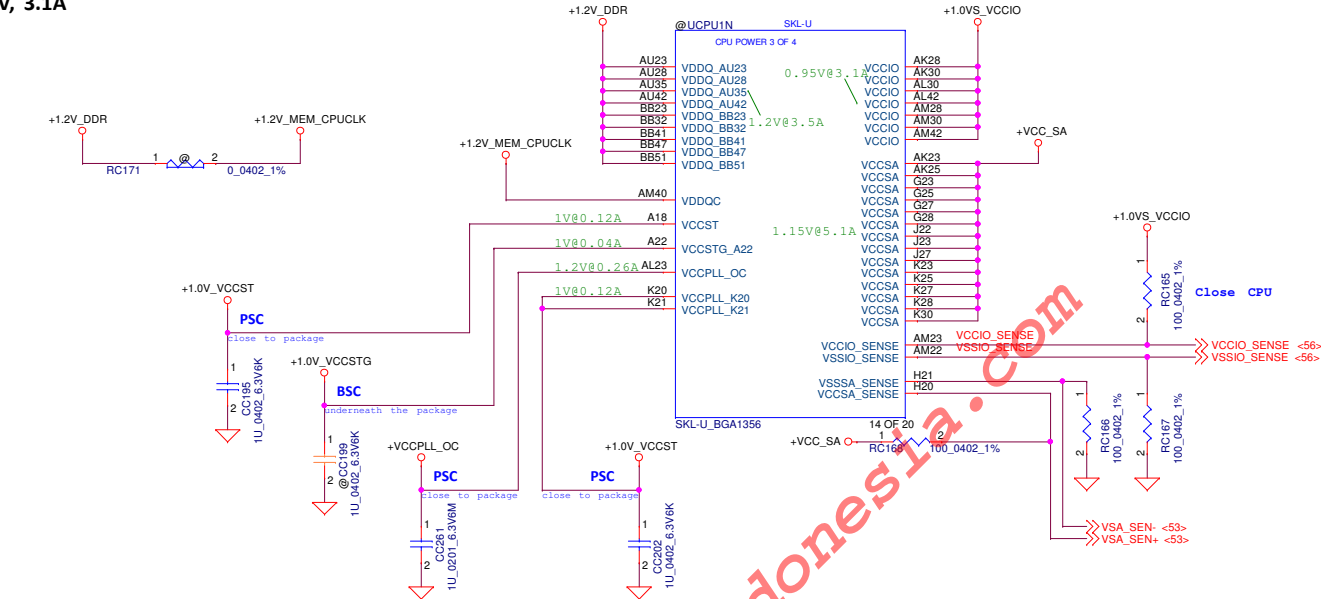


DELL CONFIDENTIAL/PROPRIETARY

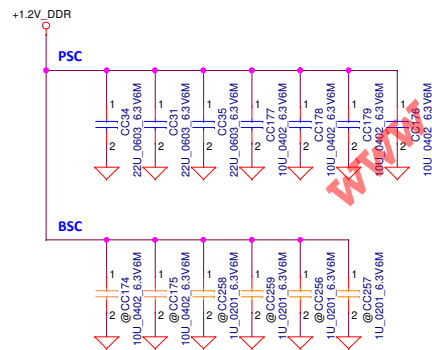
Compal Electronics, Inc.

Security Classification		Compal Secret Data		Title	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	P17-MCP(11/14)PWR-VCCGT	
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				LA-D841P	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 17 of 60			

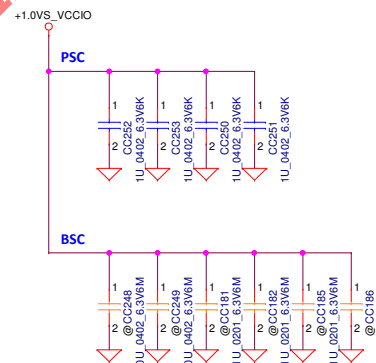
+1.2V_DDR: 1.2V, 3.5A
 +1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
 +1.0V_VCCSTG: 1V, 40mA
 +VCCPLL_OC: 1.2V, 260mA
 +1.0VS_VCCIO: 0.85~0.95V, 3.1A
 +VCC_SA: 1.15V, 5.1A



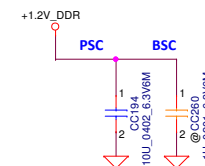
+1.2V_DDR Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (8)
 Primary Side (close to package):
 10U_0402*4 pcs + 22U_0603*3 pcs



+1.0VS_VCCIO Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (8)
 Primary Side (close to package):
 1U_0402*4 pcs



+1.2V_MEM_CPUCLK (VDDQC) Place on CPU
 Back Side (underneath the package):
 1U_0201*1 pcs (8)
 Primary Side (close to package):
 10U_0402 * 1 pcs

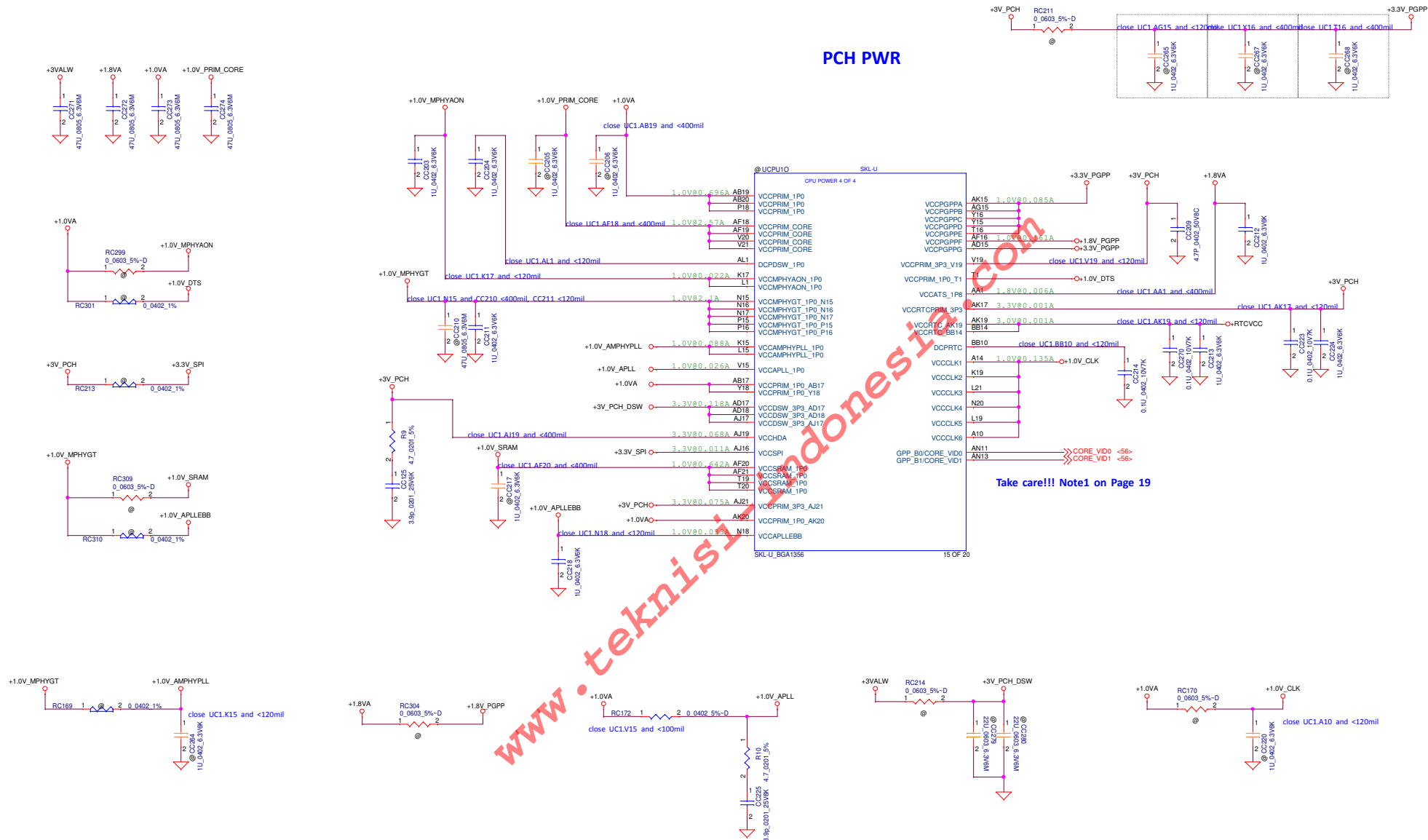


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

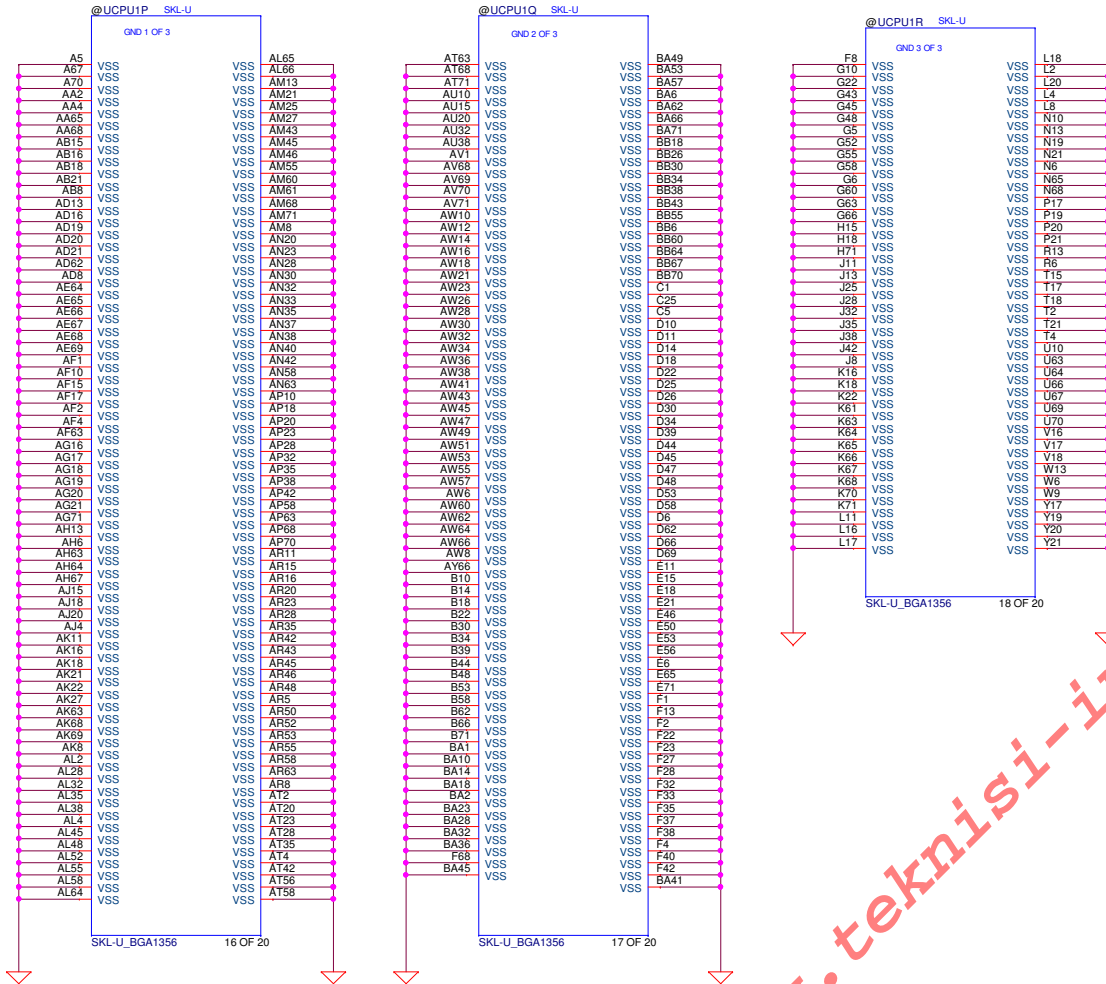
Security Classification	Compal Secret Data	
Issued Date	2015/12/16	Deciphered Date
		2016/12/13
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Title	P18-MCP(12/14)PWR-VCCIO, MEM	
Size	Document Number	Rev
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Date:	Wednesday, August 31, 2016	Sheet 18 of 60



Note1: VCCPRIM_CORE Implementat i on wá h PCH CORE_V D Reco mnendat i on

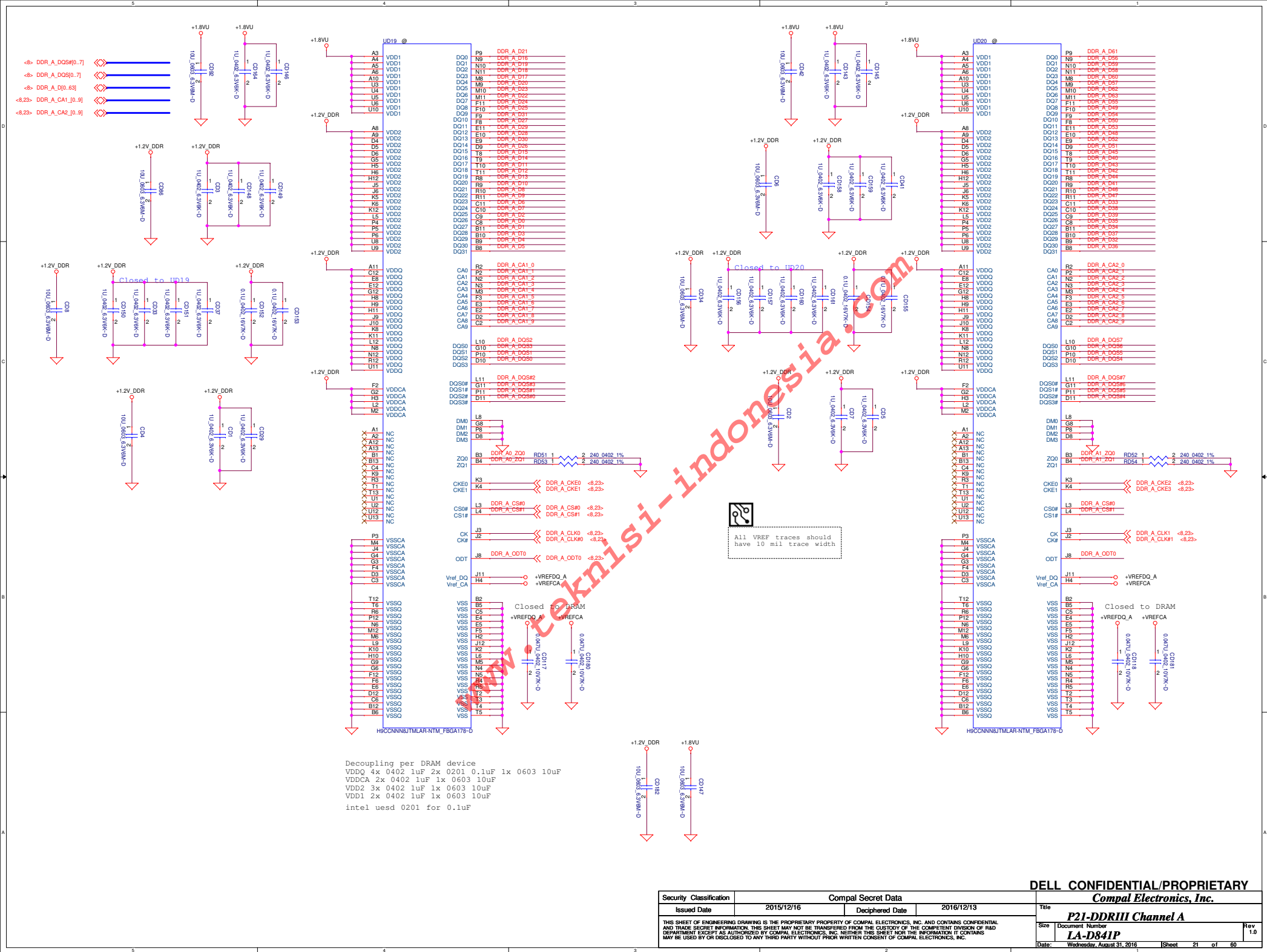
R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



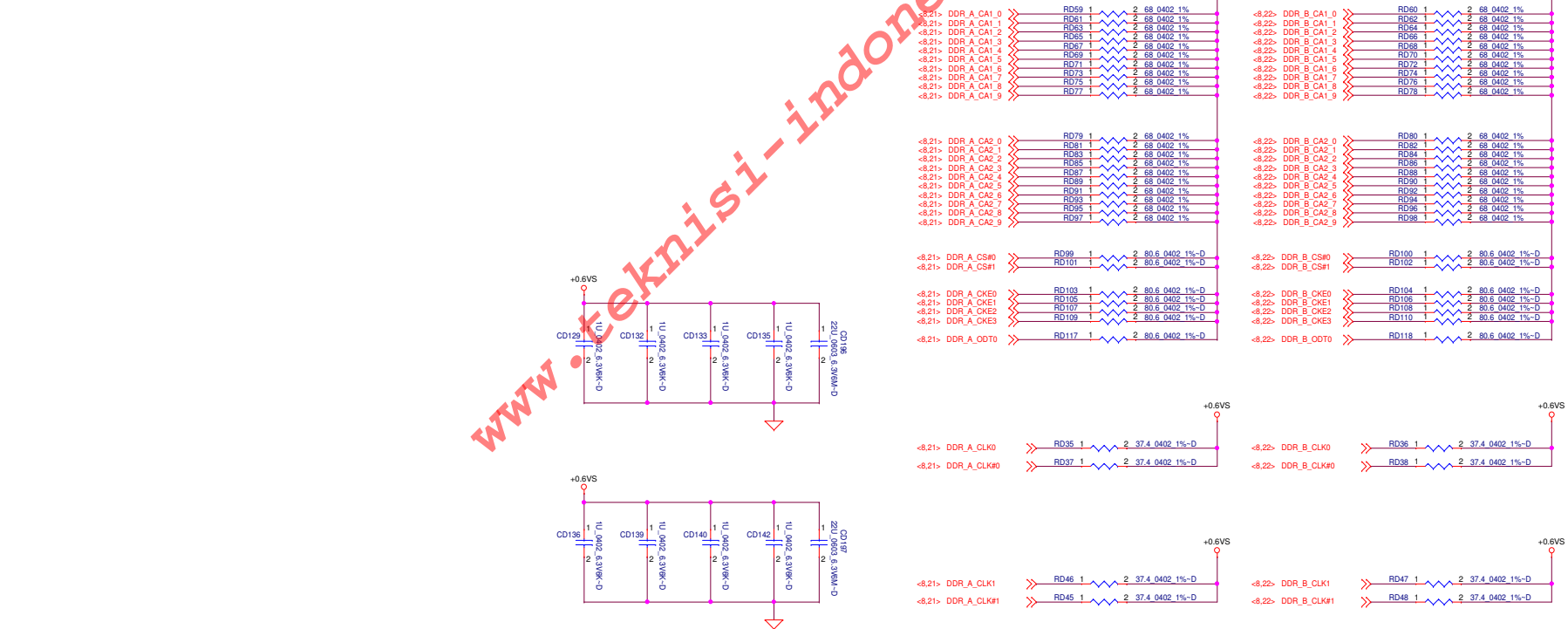
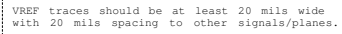
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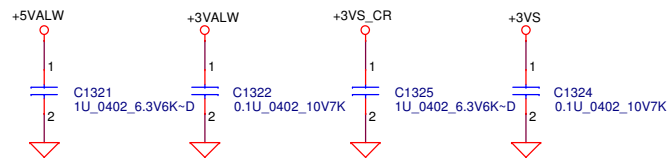
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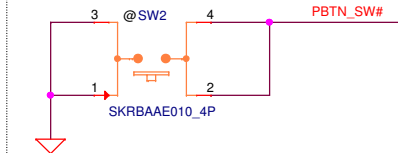
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				Document Number	Rev 1.0	
				LA-D841P		
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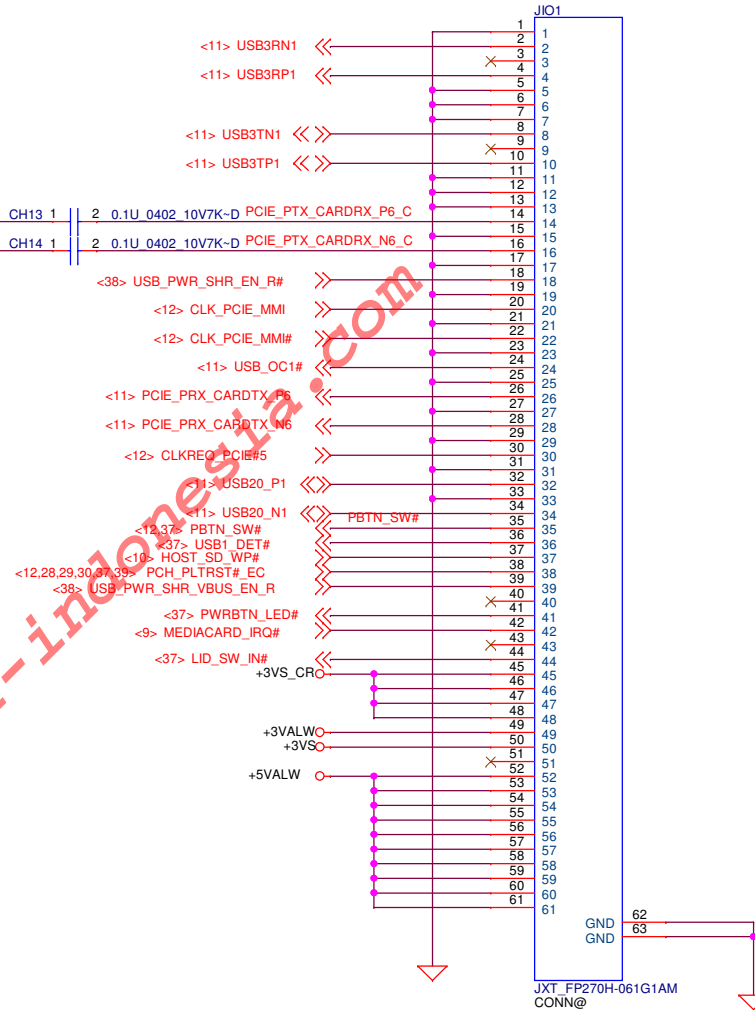


NPI Stage Power Switch



<11> PCIE_PTX_CARDRX_P6
<11> PCIE_PTX_CARDRX_N6

CH13 1 2 0.1U 0402 10V7K-D PCIE_PTX_CARDRX_P6_C
CH14 1 2 0.1U 0402 10V7K-D PCIE_PTX_CARDRX_N6_C



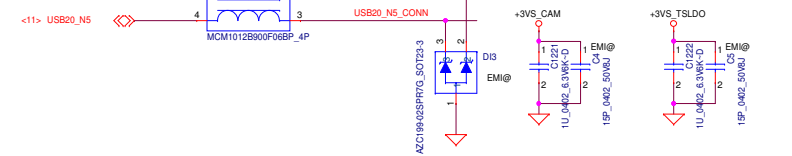
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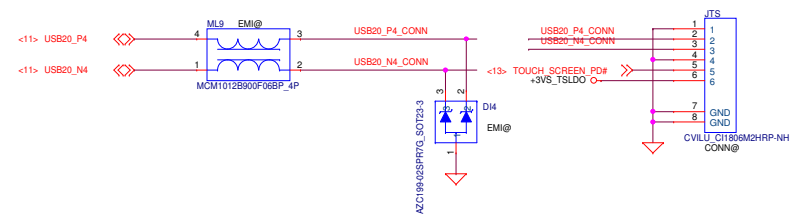
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Camera + Touch Screen

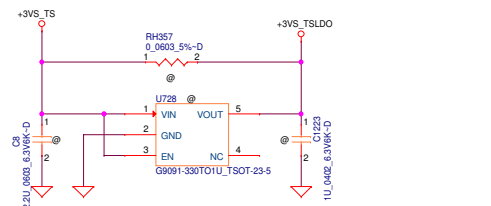
Camera



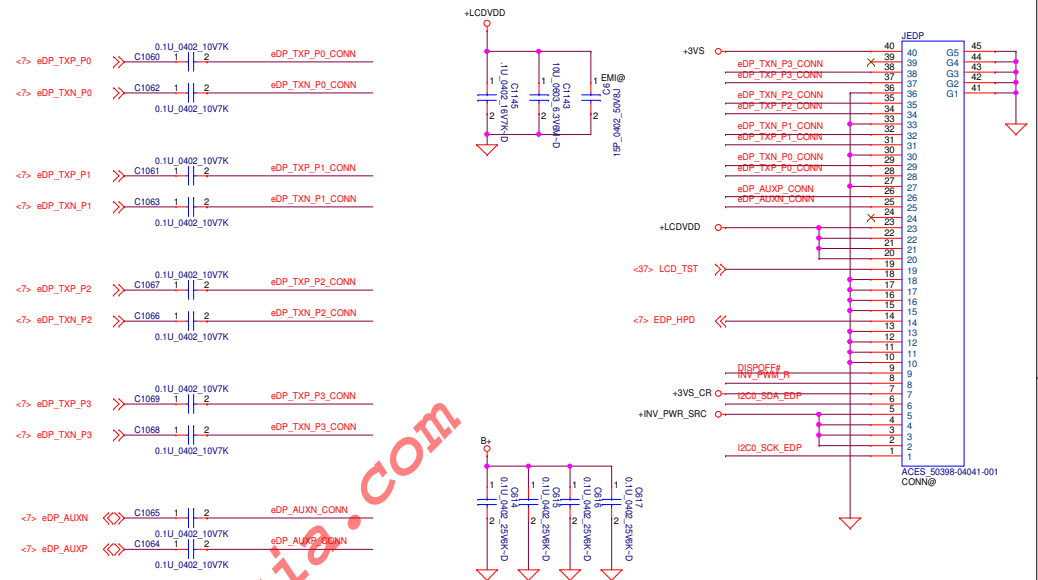
Touch Screen



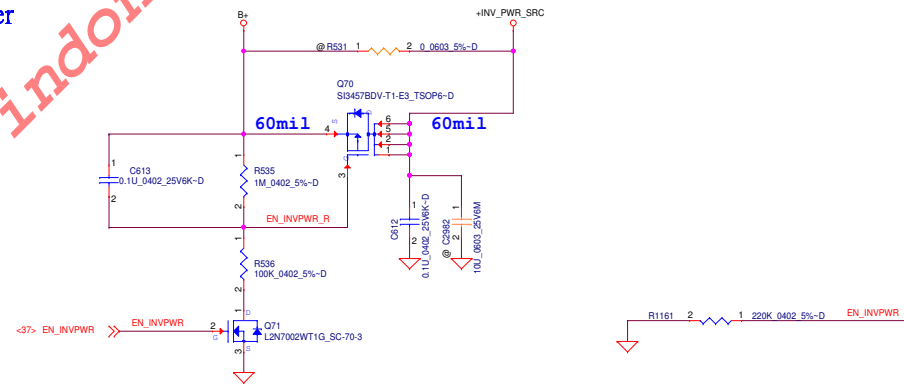
Touch Screen LDO



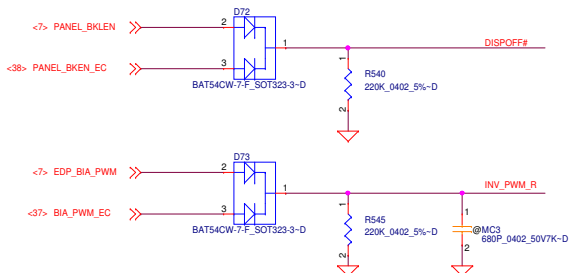
eDP Conn



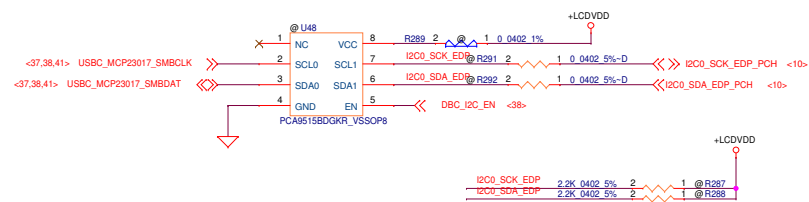
eDP BackLight Power



BackLight PWM Control



DBC delay schematic

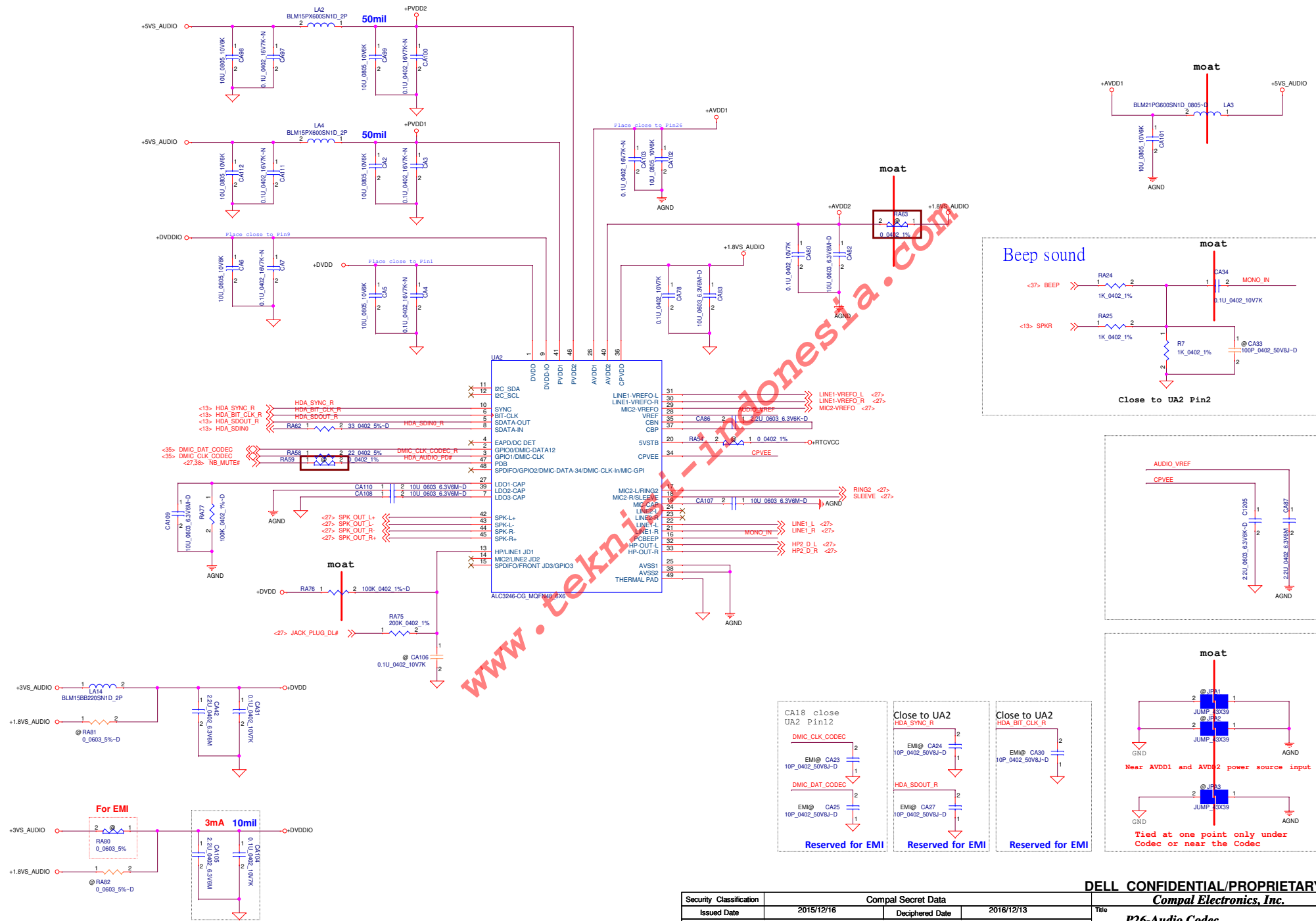


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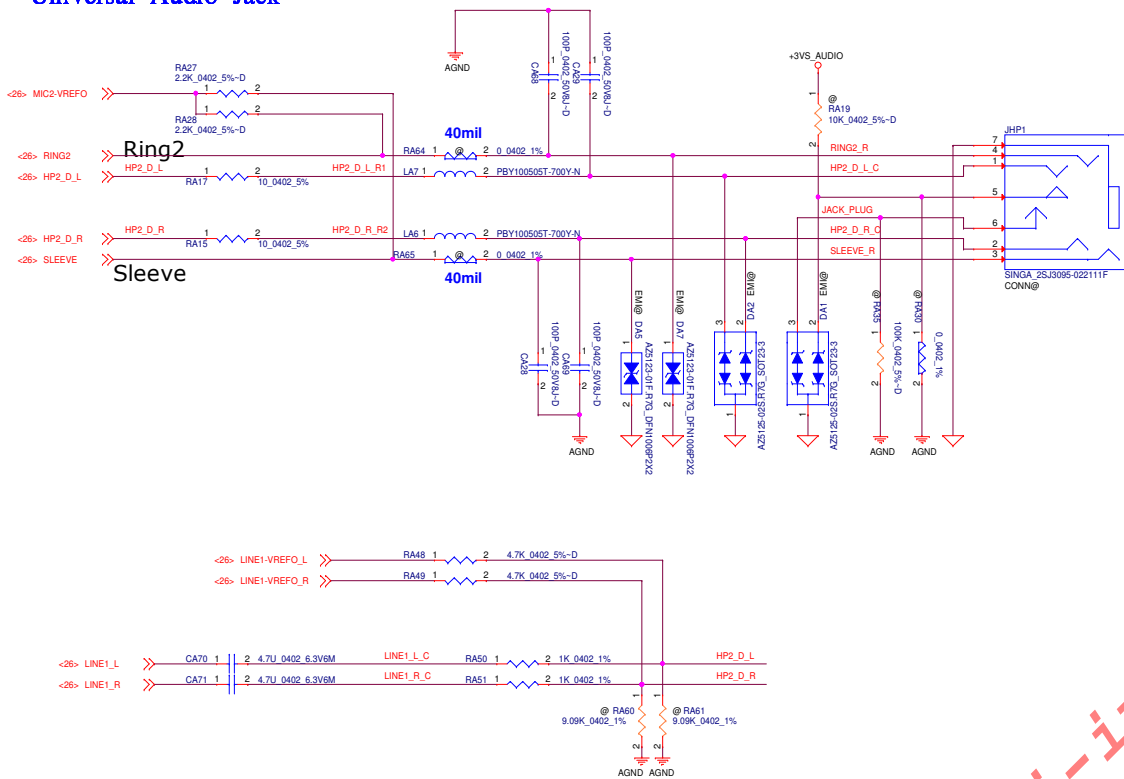
Compal Electronics, Inc.

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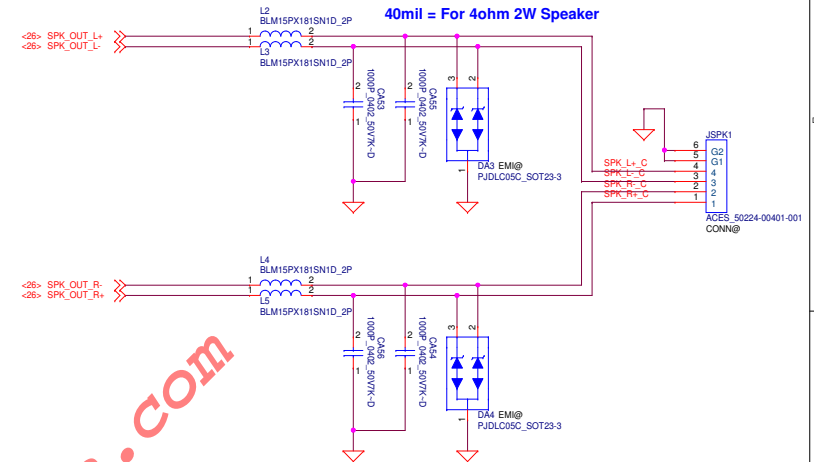
HD Audio Codec



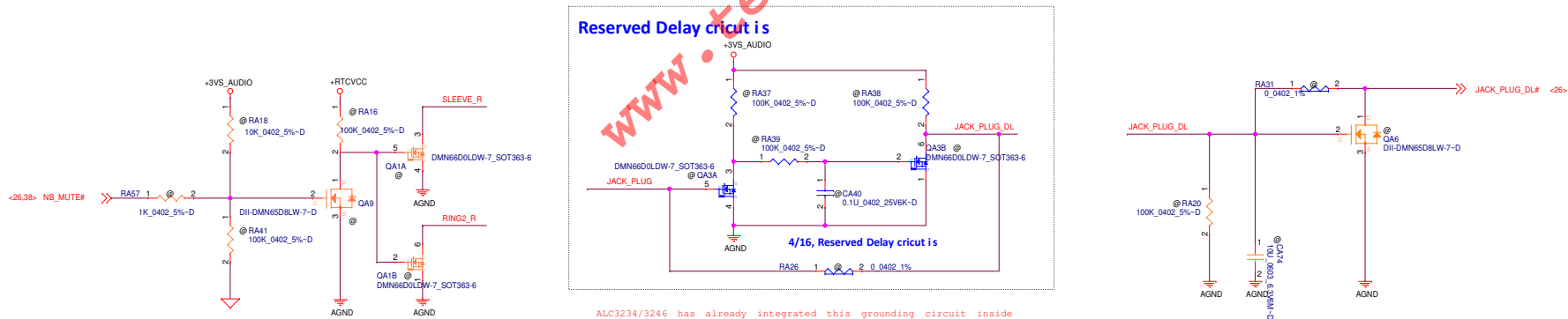
Universal Audio Jack



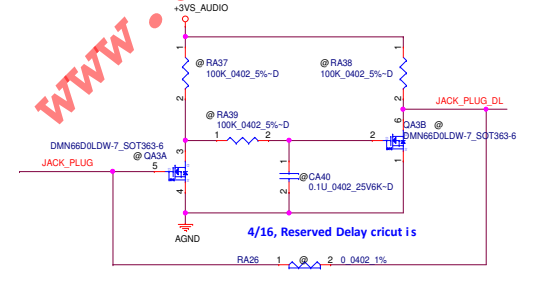
Int. Speaker Conn.



Prevent S3/S4/S5 Background Noise.



Reserved Delay circuit is



ALC3234/3246 has already integrated this grounding circuit inside the pin20

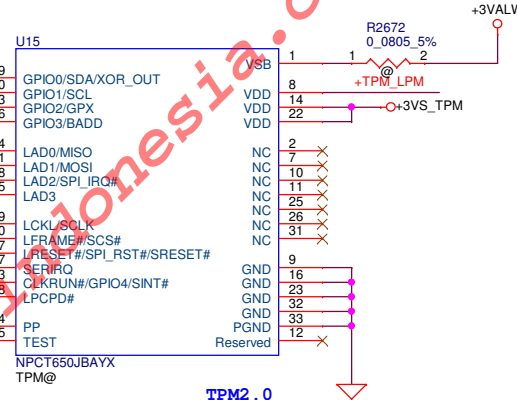
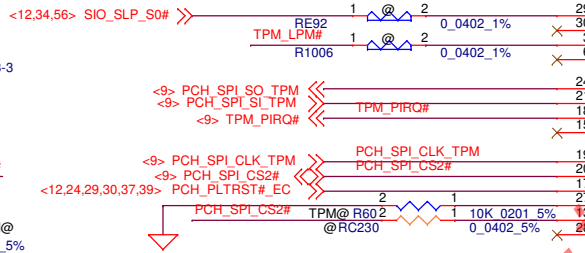
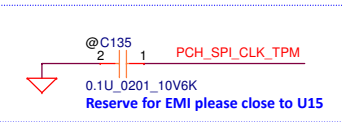
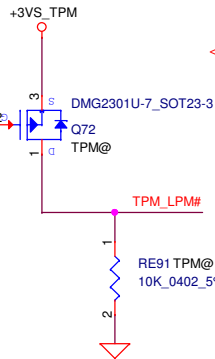
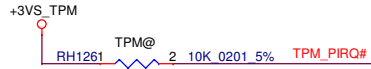
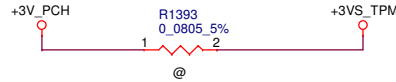
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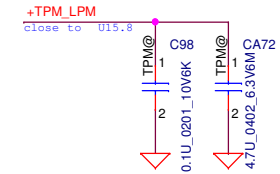
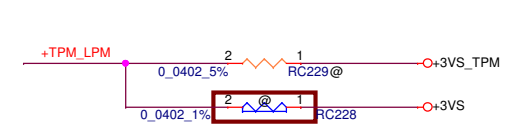
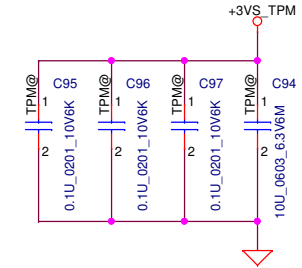
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		P27-Audio Jack / Speaker
		Size
		LA-D841P
		Rev
		1.0
		Date: Wednesday, August 31, 2016
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TPM

NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide



NOTE:
Place 0.1 uF capacitors as close as
possible to the device power pins

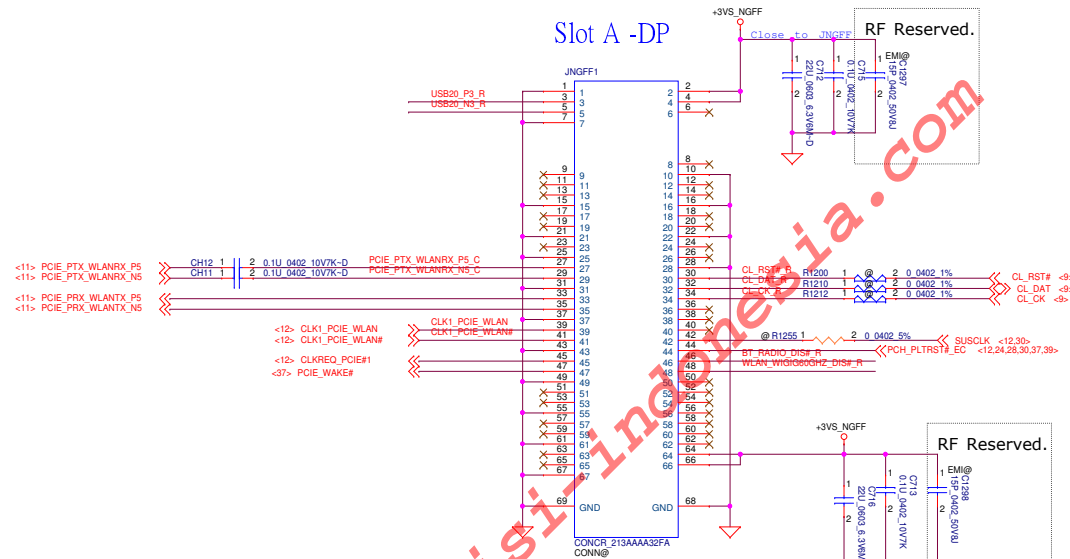
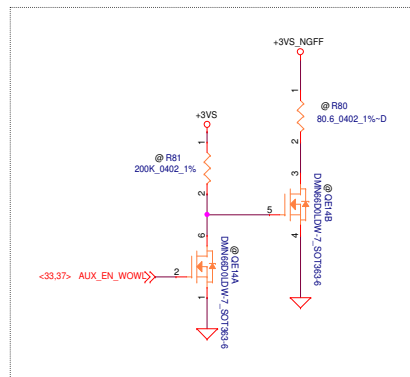
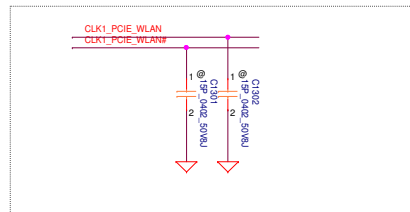
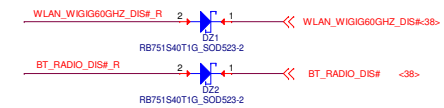
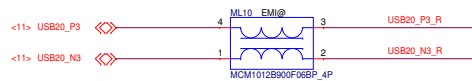


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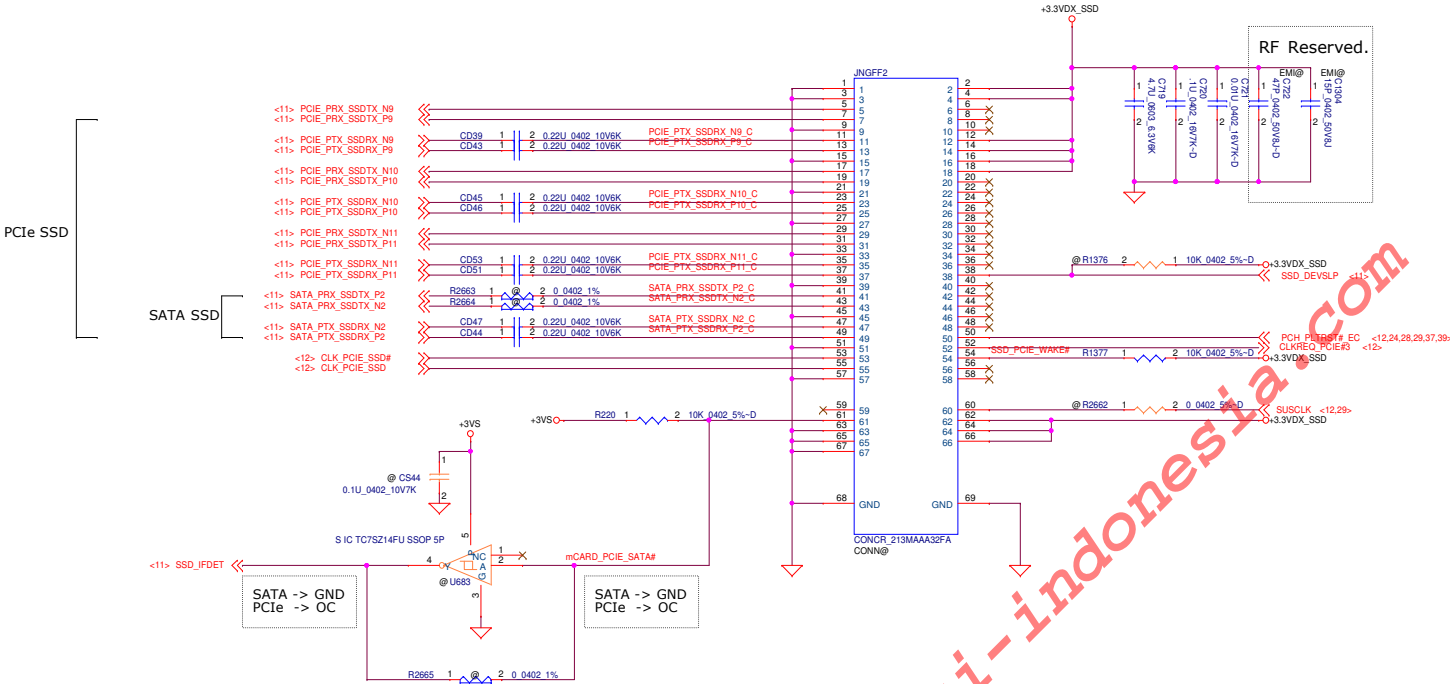
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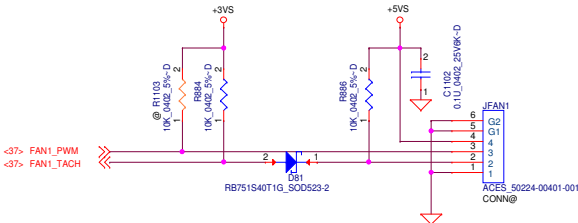
M.2 Slot-A Key-A (WLAN)



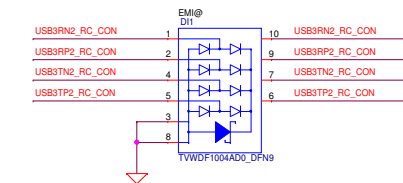
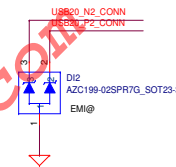
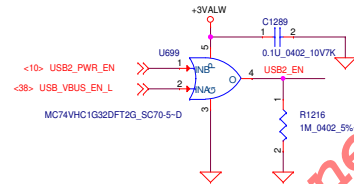
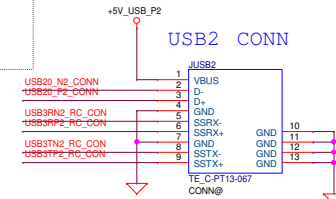
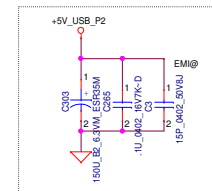
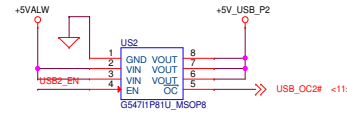
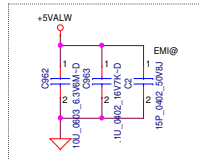
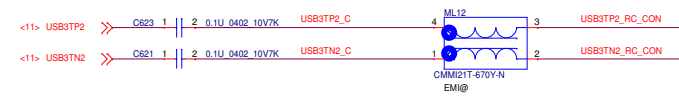
M.2 Slot-C Key-M (SSD)



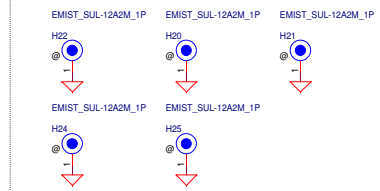
FAN CONN



USB IO Port

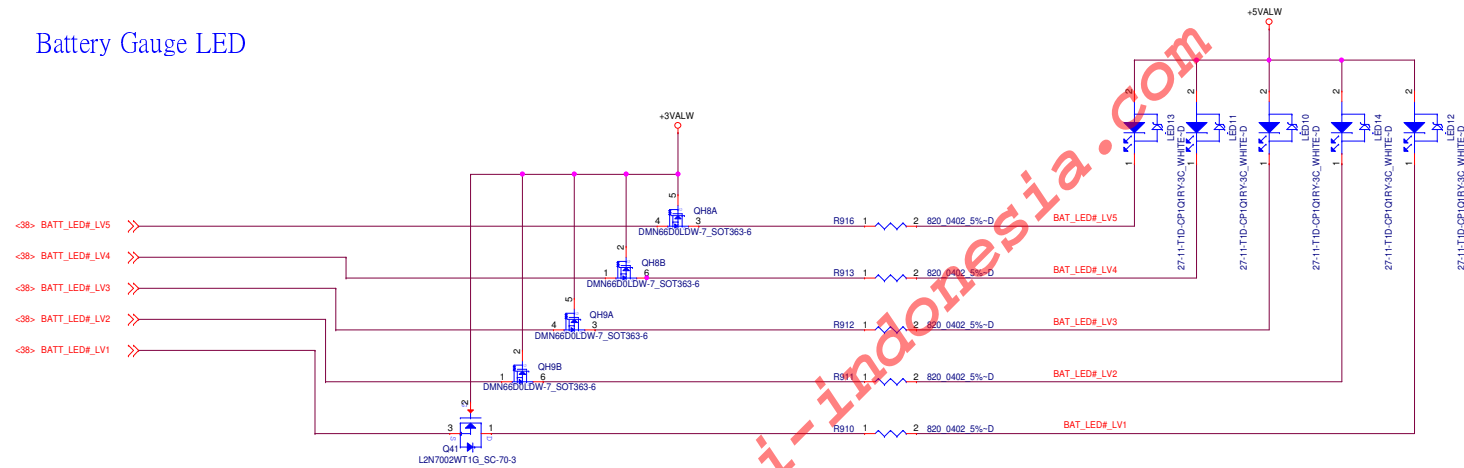


USB3.0 Shielding Clip

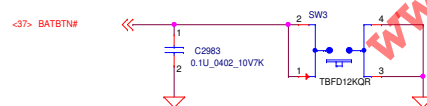


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								Document Number			
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								Date: Wednesday, August 31, 2016			
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								Rev 1.0			

Battery Gauge LED



Battery Gauge Button

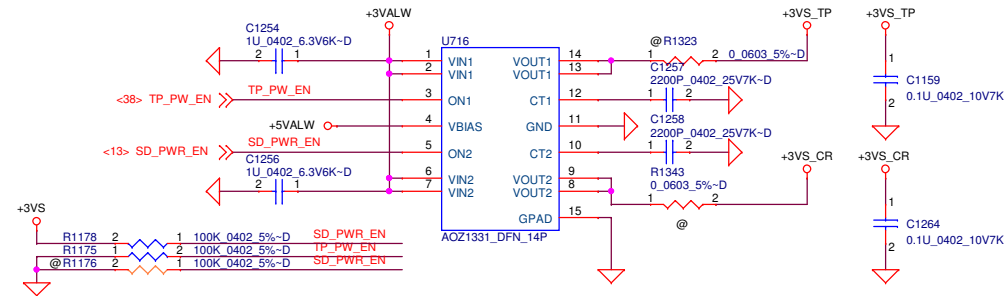


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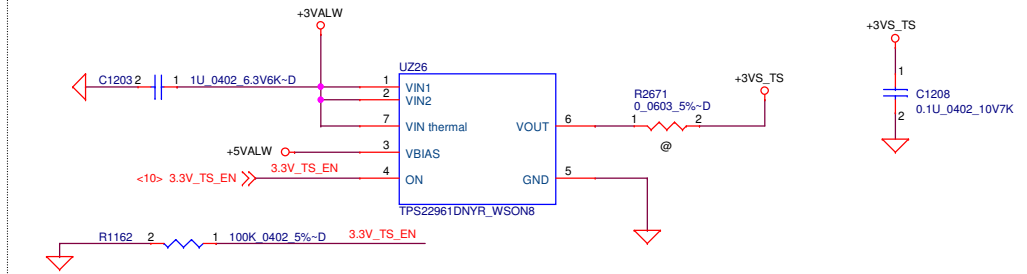
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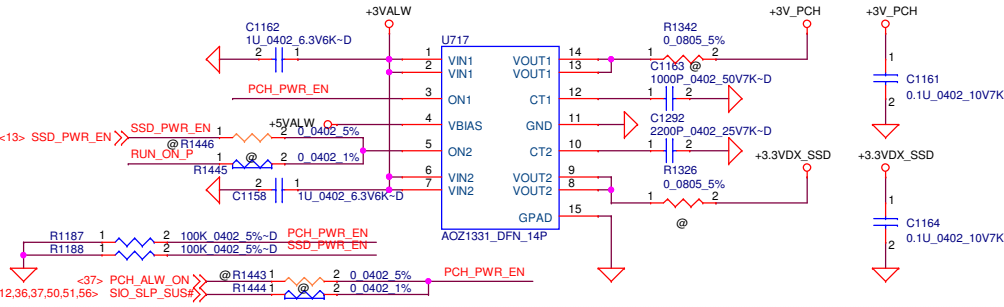
Touch Pad, Card Reader Load Switch



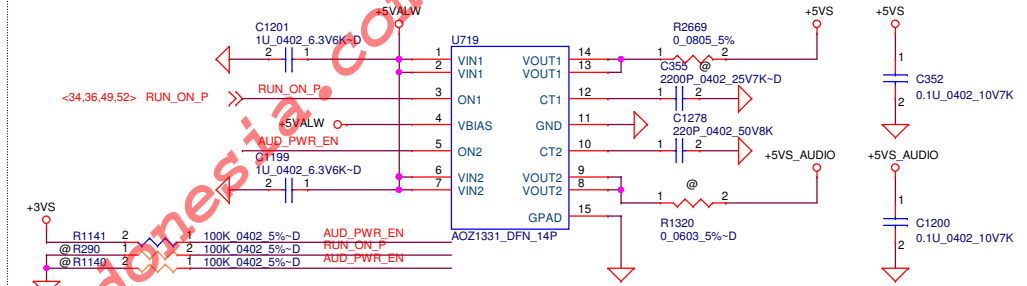
Touch Screen Load Switch



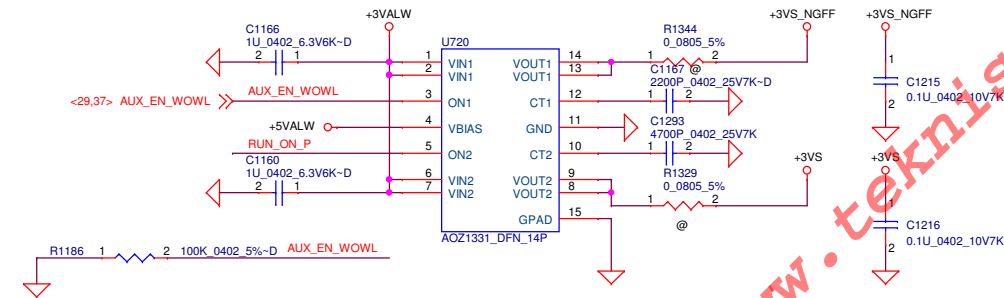
Deeper Sleep, SSD Load Switch



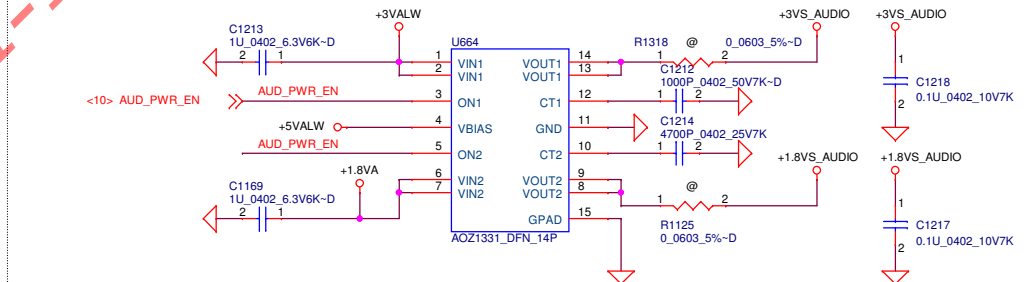
5V_Run, 5V_Audio Load Switch



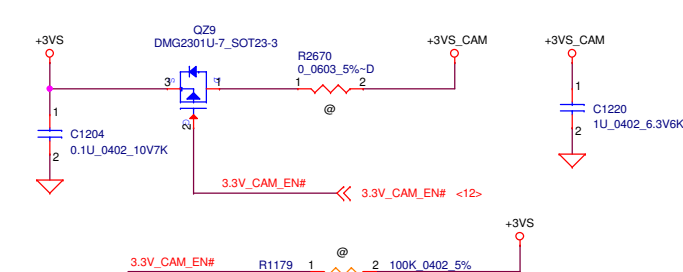
WiFi, 3V_RUN Load Switch



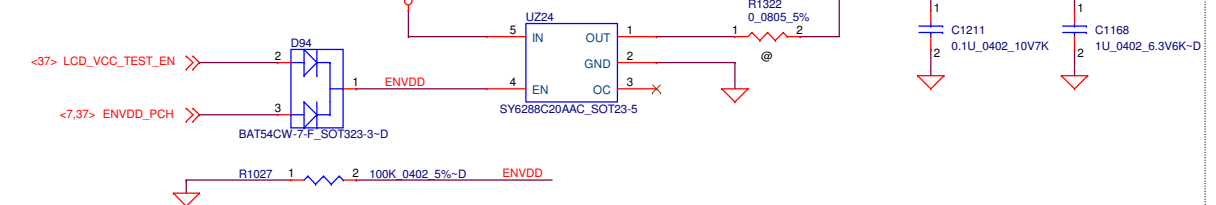
3V_Audio, 1.8V_Audio Load Switch



Camera



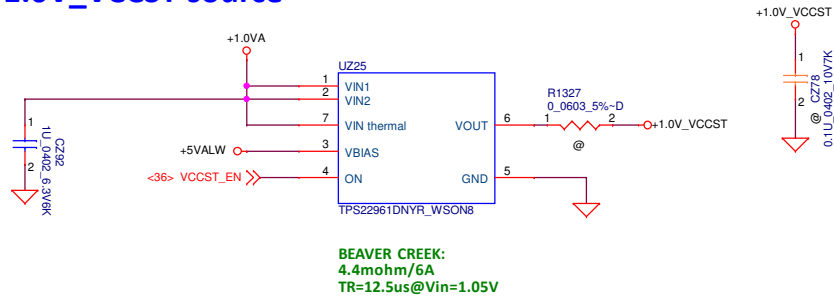
LCD Load Switch



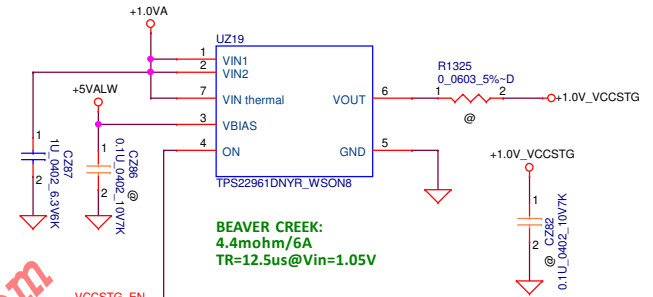
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								Document Number			
								LA-D841P			
								Rev			
								1.0			
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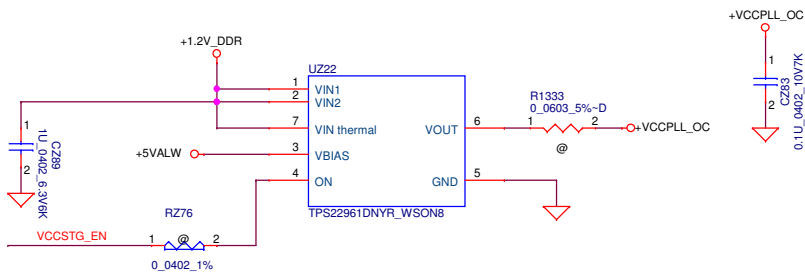
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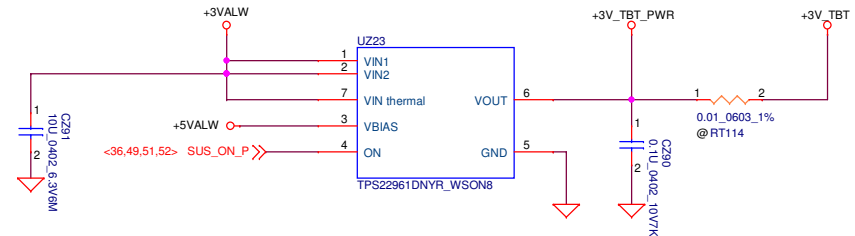
+1.0V_VCCSTG source



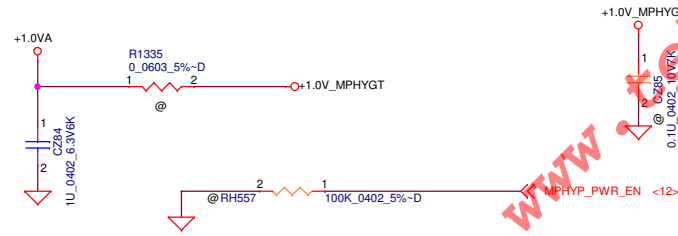
+VCCPLL_OC source



TBT Power circuits



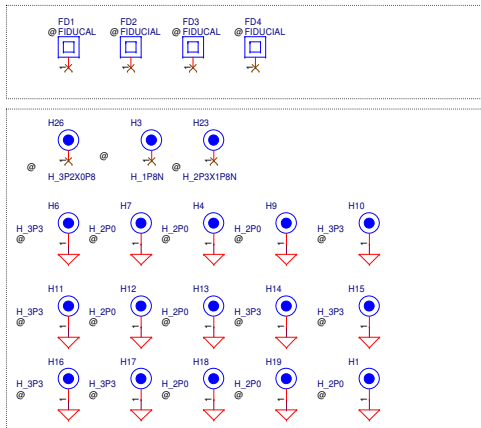
+1.0V_MPHYGT source



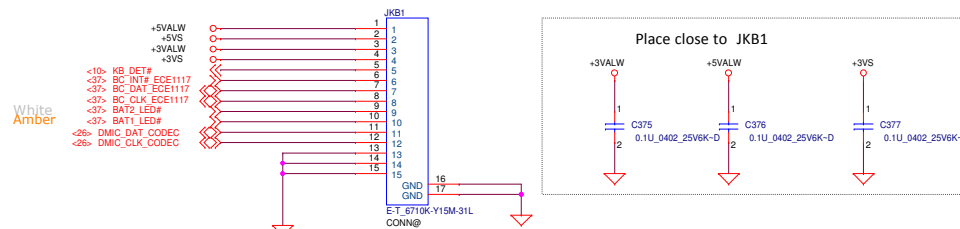
	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

Security Classification	Compal Secret Data		
Issued Date	2015/12/16	Deciphered Date	2016/12/13
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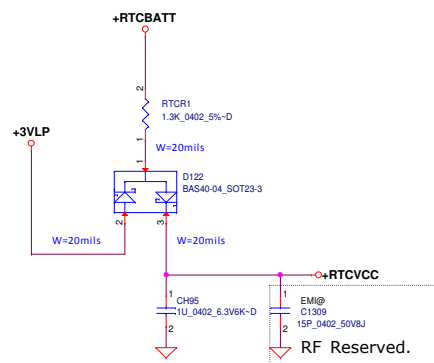
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title P34-DC/DC Interface 2			
Size	Document	Number	Rev
		LA-D841P	1.0
Date:	Wednesday, August 31, 2016	Sheet	34 of 60



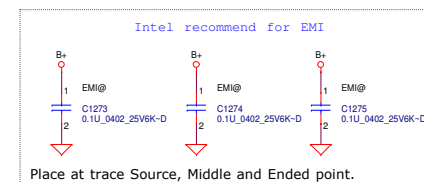
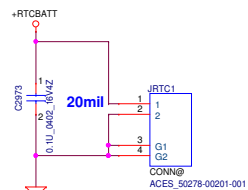
Keyboard Controller board + DMIC



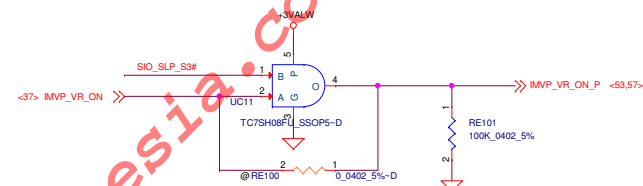
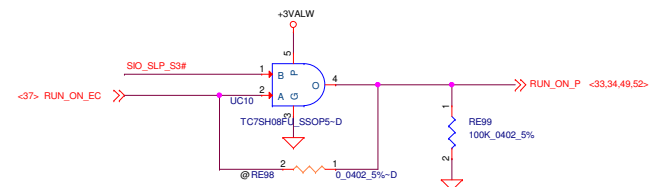
RTC Battery With Charge Function



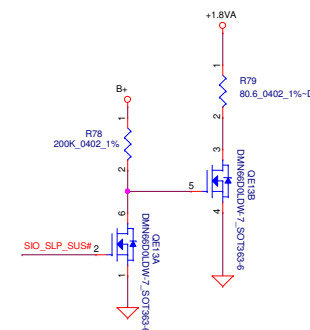
RTC Battery Conn



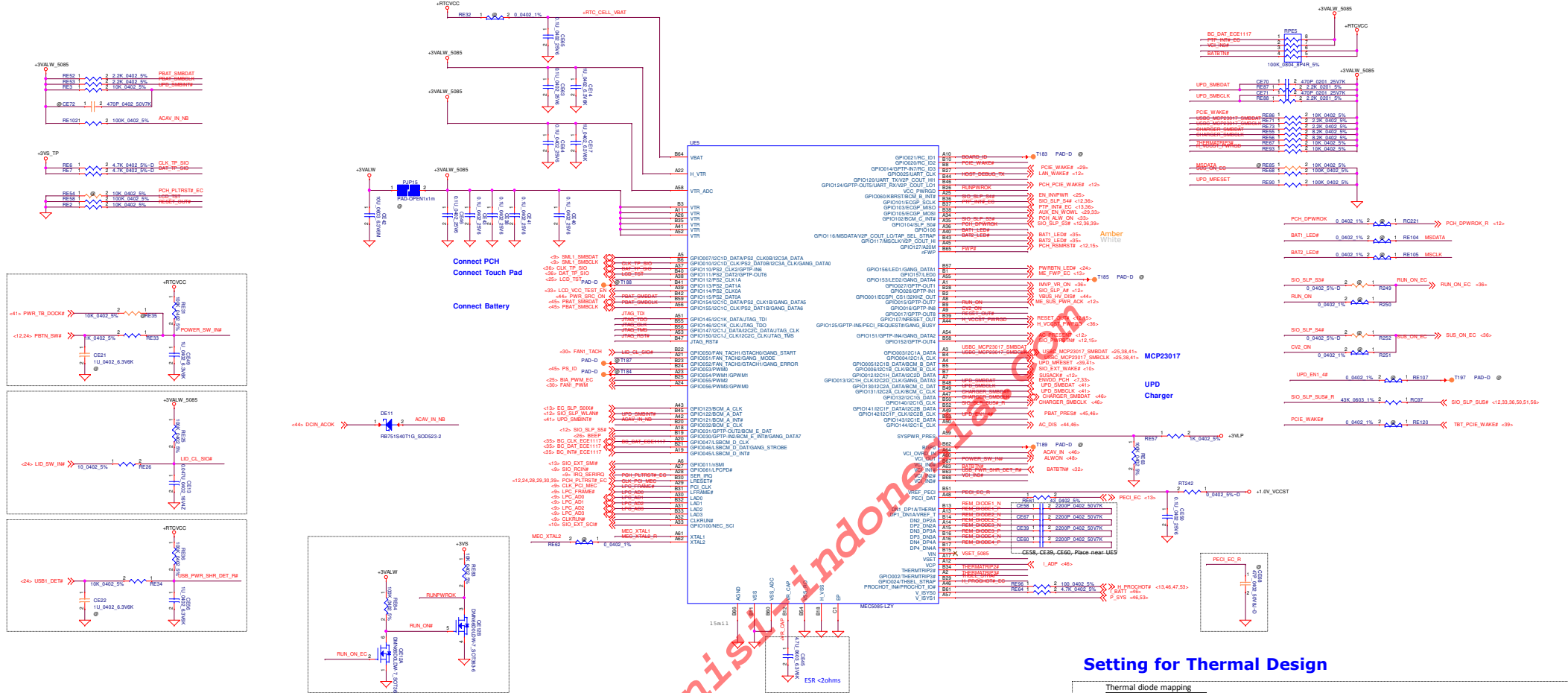
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				Size	Document Number
				LA-D841P	
				Date:	Rev
				Wednesday, August 31, 2016	1.0
				Sheet	35 of 60



+1.8VA Discharge



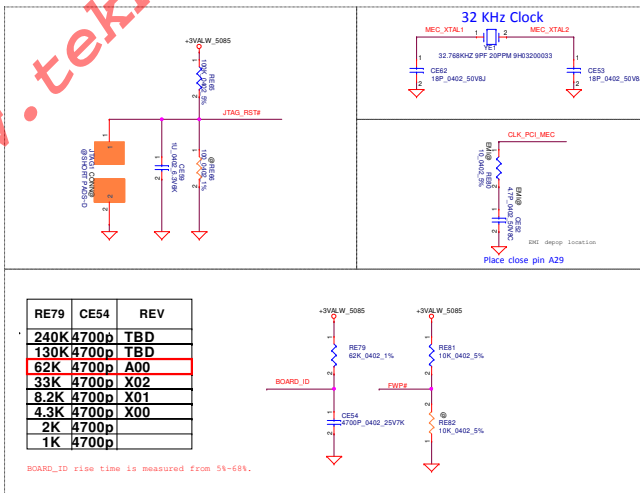
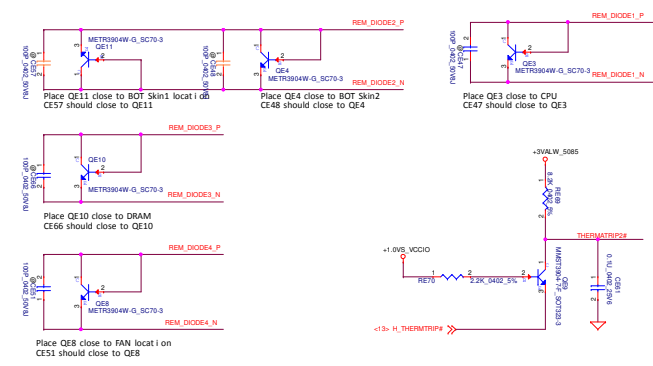
Security Classification		Compal Secret Data		CONFIDENTIAL/PROPRIETARY	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	Compal Electronics, Inc.	
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				P36-TP/PWERGDL/LID	
				LA-D84IP	
		Size	Document Number	Rev	
		Date:	Wednesday, August 31, 2016	Sheet	36 of 60



Setting for Thermal Design

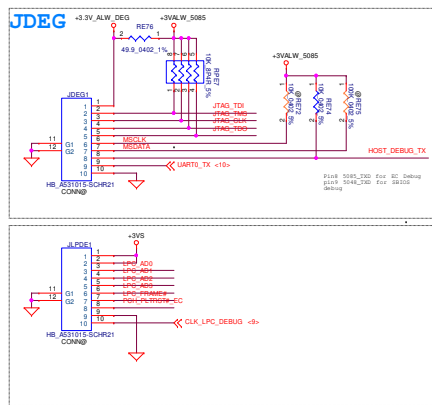
5085 Channel	Locat i on
DP1/DN1	CPU(OTP)
DP2/DN2	BOT Skin2
DN2A/DP2A	BOT Skin1
DP3/DN3	DRAM
DP4/DN4	FAN

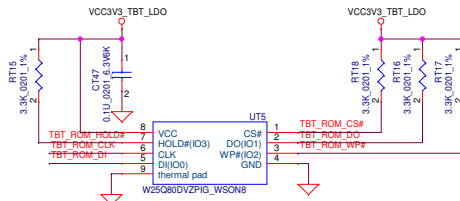
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings



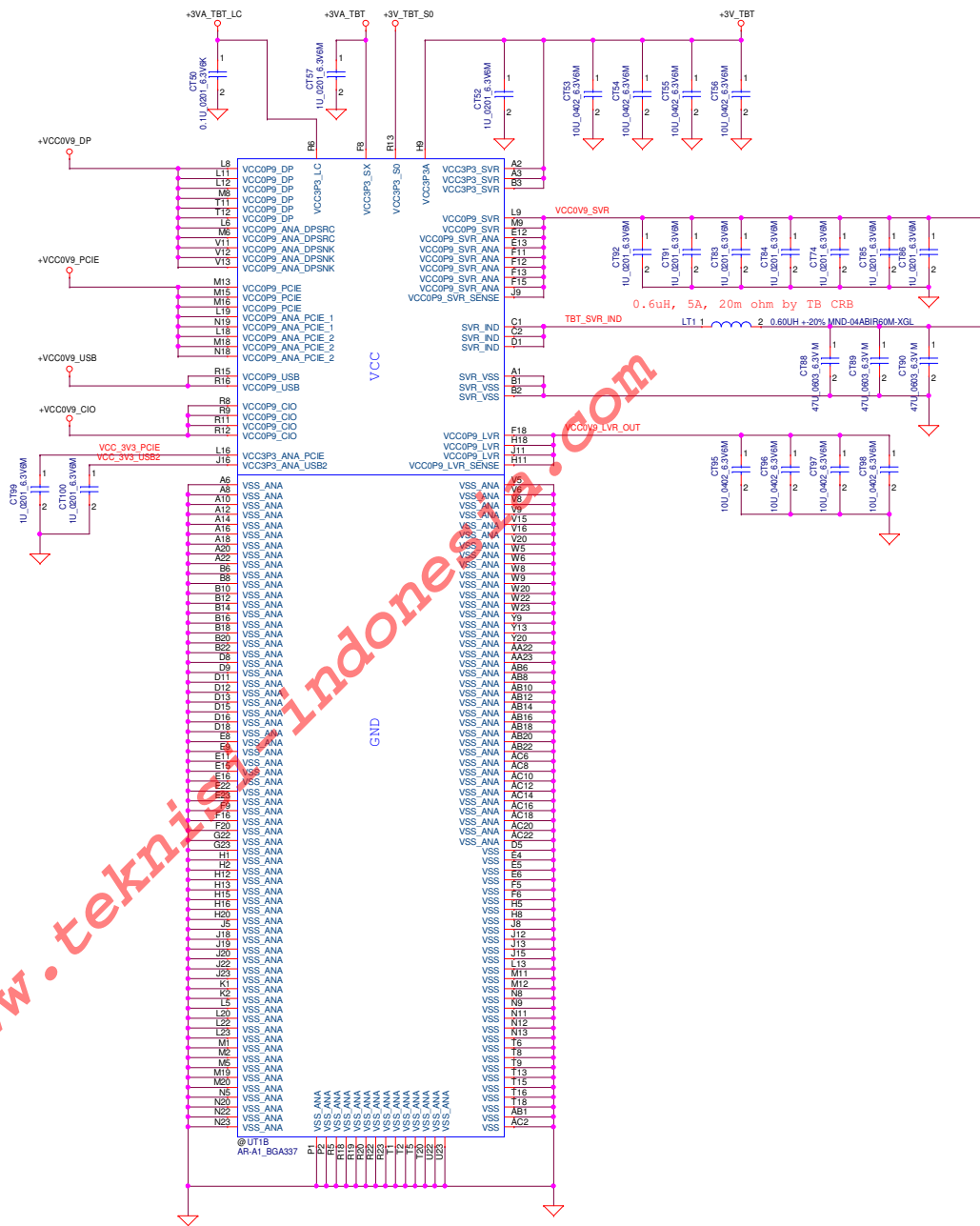
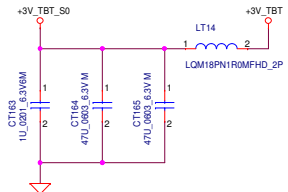
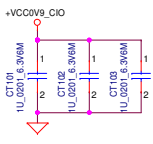
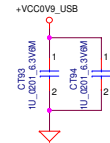
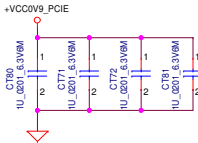
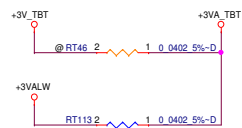
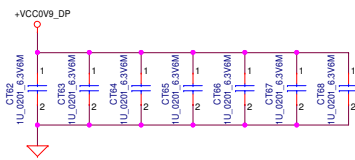
RE79	CE54	REV
240K 4700p	TBD	
130K 4700p	TBD	
62K 4700p	A00	
33K 4700p	X02	
8.2K 4700p	X01	
4.3K 4700p	X00	
2K 4700p		
1K 4700p		

BOARD_Rise time is measured from 5%-68%.



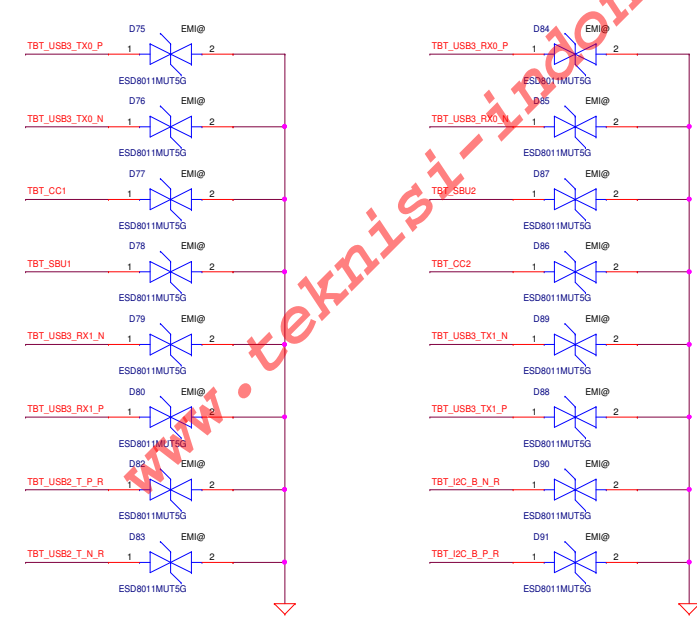
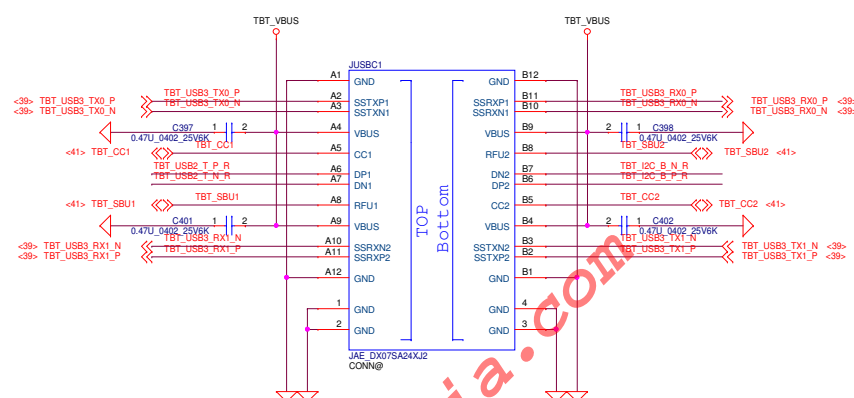
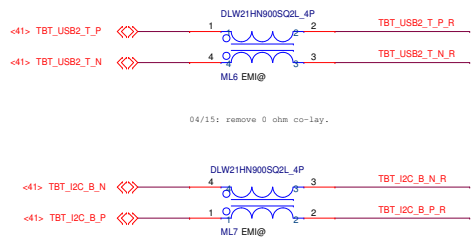


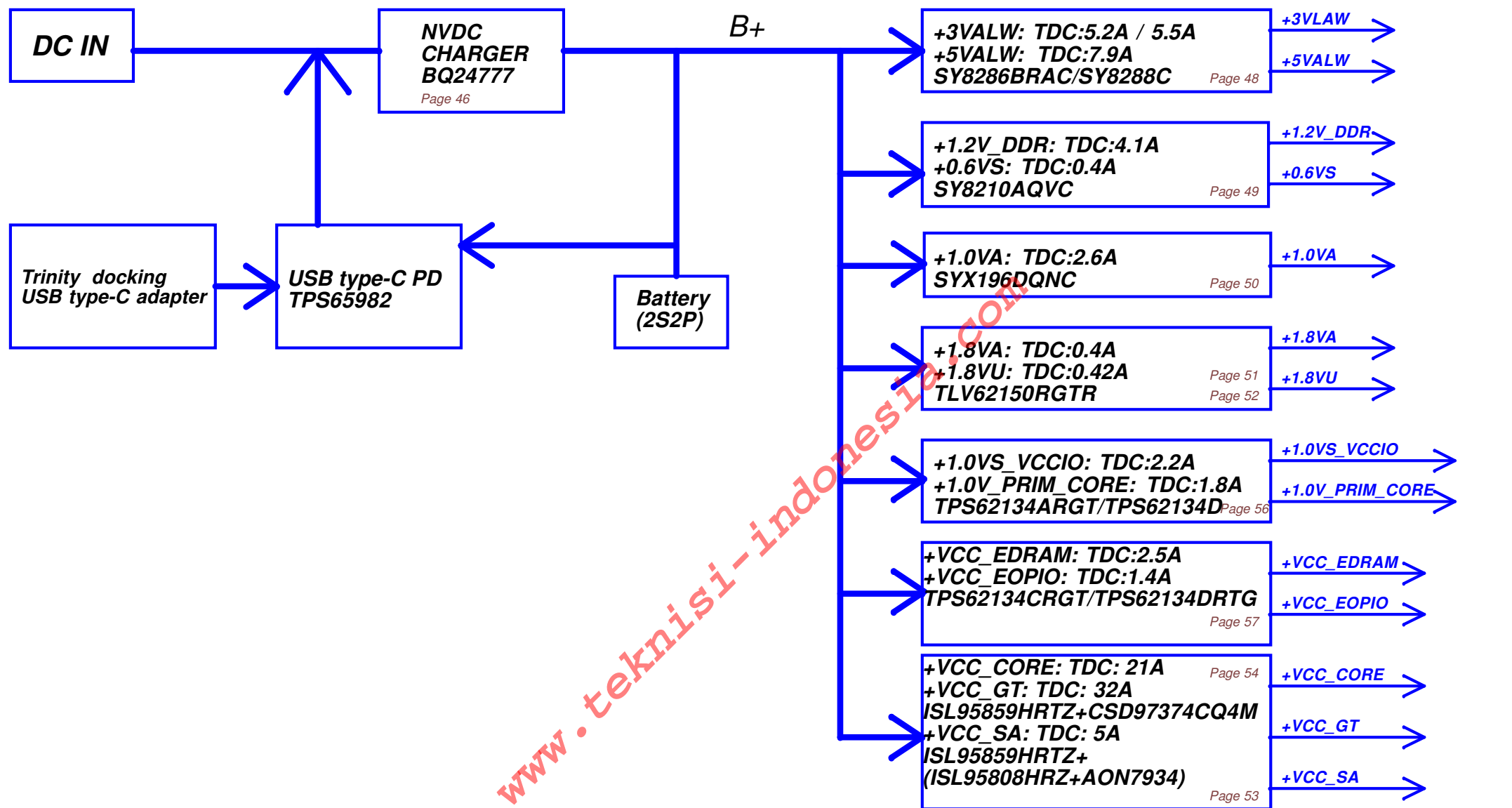
Date: Wednesday, August 31, 2016 Sheet 39 of 60



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2015/12/16		2016/12/13		P40-AR TBT (2/2) PWR / VSS	
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				Document Number	
				LA-D841P	
				Rev	
				1.0	
				Date: Wednesday, August 31, 2016	
				Sheet 40 of 60	





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					Size	Document Number	Rev
					LAD841P		1.0
					Date:	Wednesday, August 31, 2016	Sheet 43 of 59

Remove source back function

B+ Power

S9

P-MOSFET

ACN8409 DFN6-8

PR209

100K_0402_1%

PR210

100K_0402_1%

PR211

100K_0402_1%

PR212

100K_0402_1%

PR213

100K_0402_1%

PR214

100K_0402_1%

PR215

100K_0402_1%

PR216

100K_0402_1%

PR217

100K_0402_1%

PR218

100K_0402_1%

PR219

100K_0402_1%

PR220

100K_0402_1%

PR221

100K_0402_1%

PR222

100K_0402_1%

PR223

100K_0402_1%

PR224

100K_0402_1%

PR225

100K_0402_1%

PR226

100K_0402_1%

PR227

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PR228

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PR229

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PR230

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PR231

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PR234

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PR301

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PR330

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PR331

100K_0402_1%

PR332

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PR333

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PR334

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PR335

100K_0402_1%

PR336

100K_0402_1%

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PR338

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PR339

100K_0402_1%

PR340

100K_0402_1%

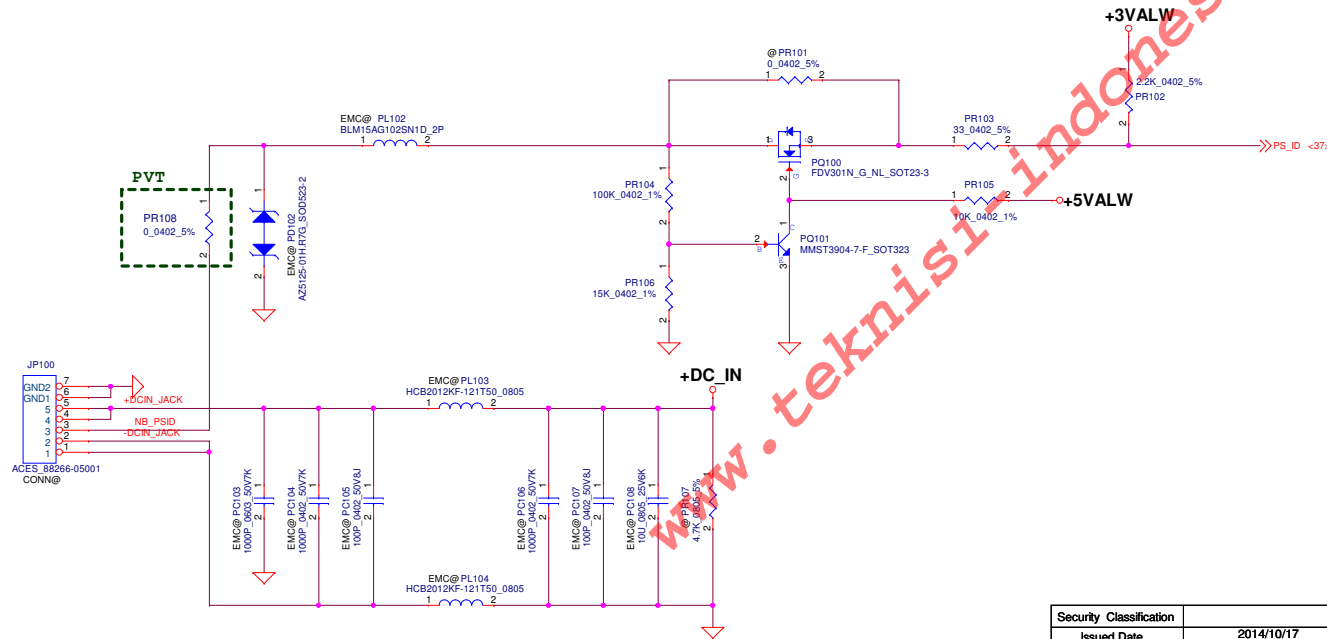
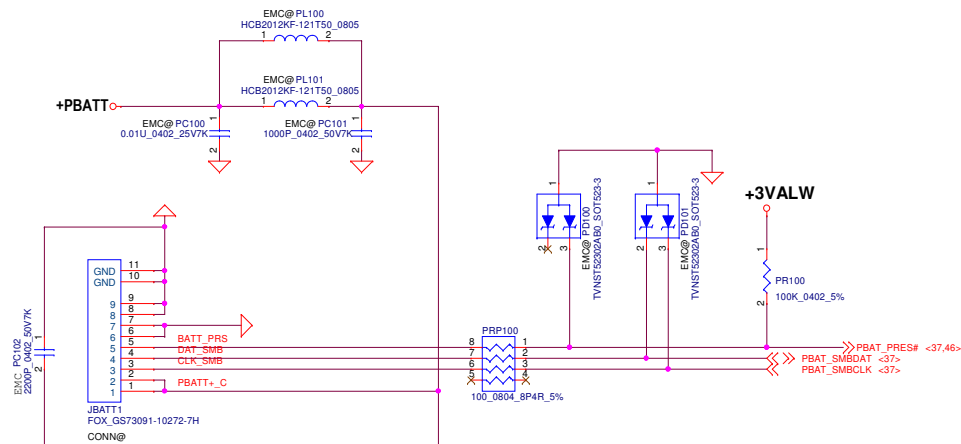
PR341

PBATT1 connector

SMART

Battery:

- 1.BATT++
- 2.BATT++
- 3.CLK_SMB
- 4.DAT_SMB
- 5.BAT_PRS
- 6.SYS_PRES
- 7.BAT_ALERT
- 8.GND
- 10.GND
- 11.GND



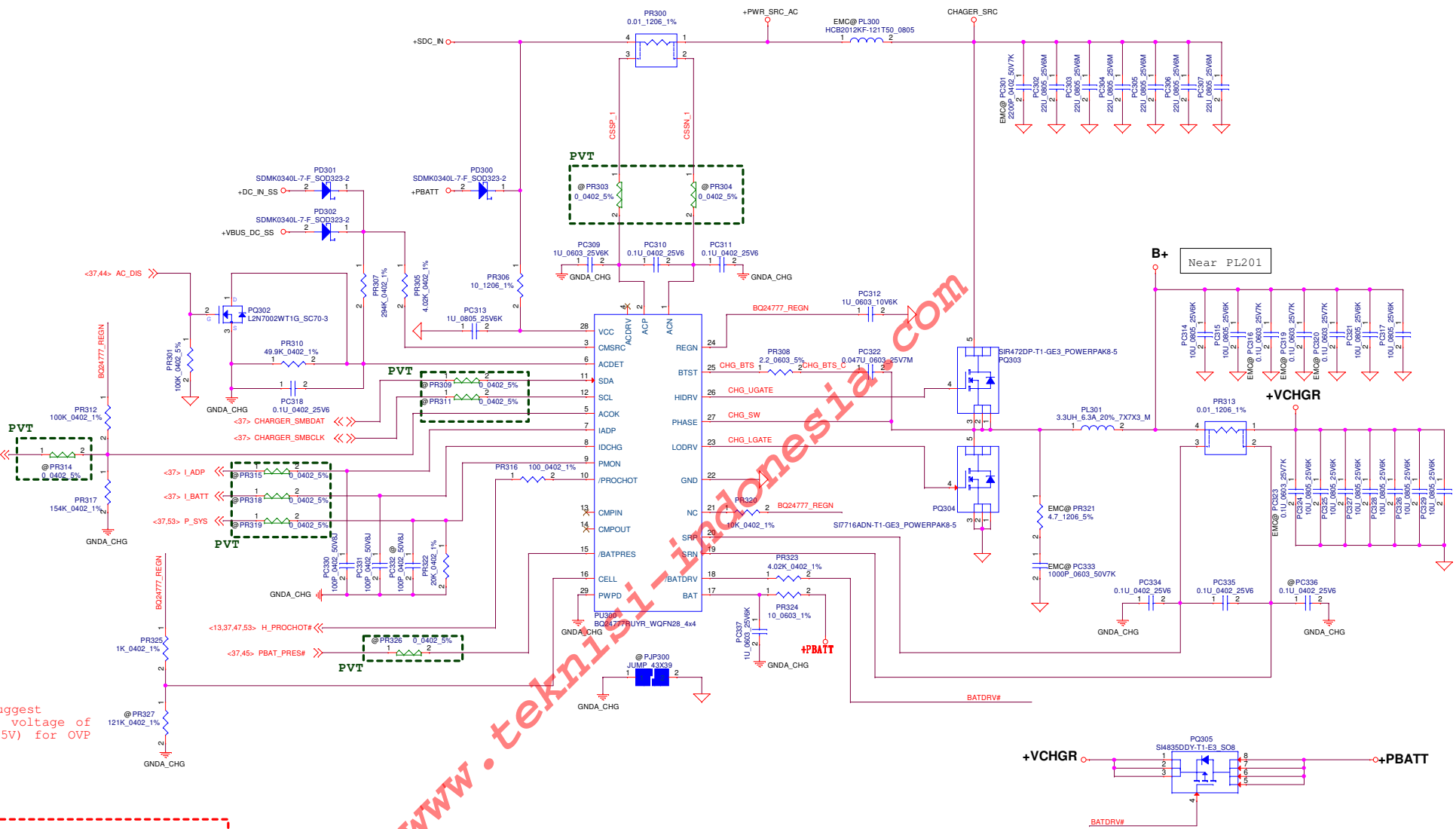
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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Date:	Wednesday, August 31, 2016	Sheet	45	of 59

PQ302
main:SB00000ST00
2nd:SB00000U000
3rd:SB00000Z600

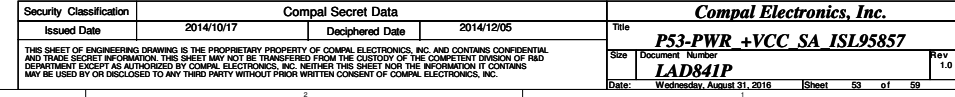
CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side

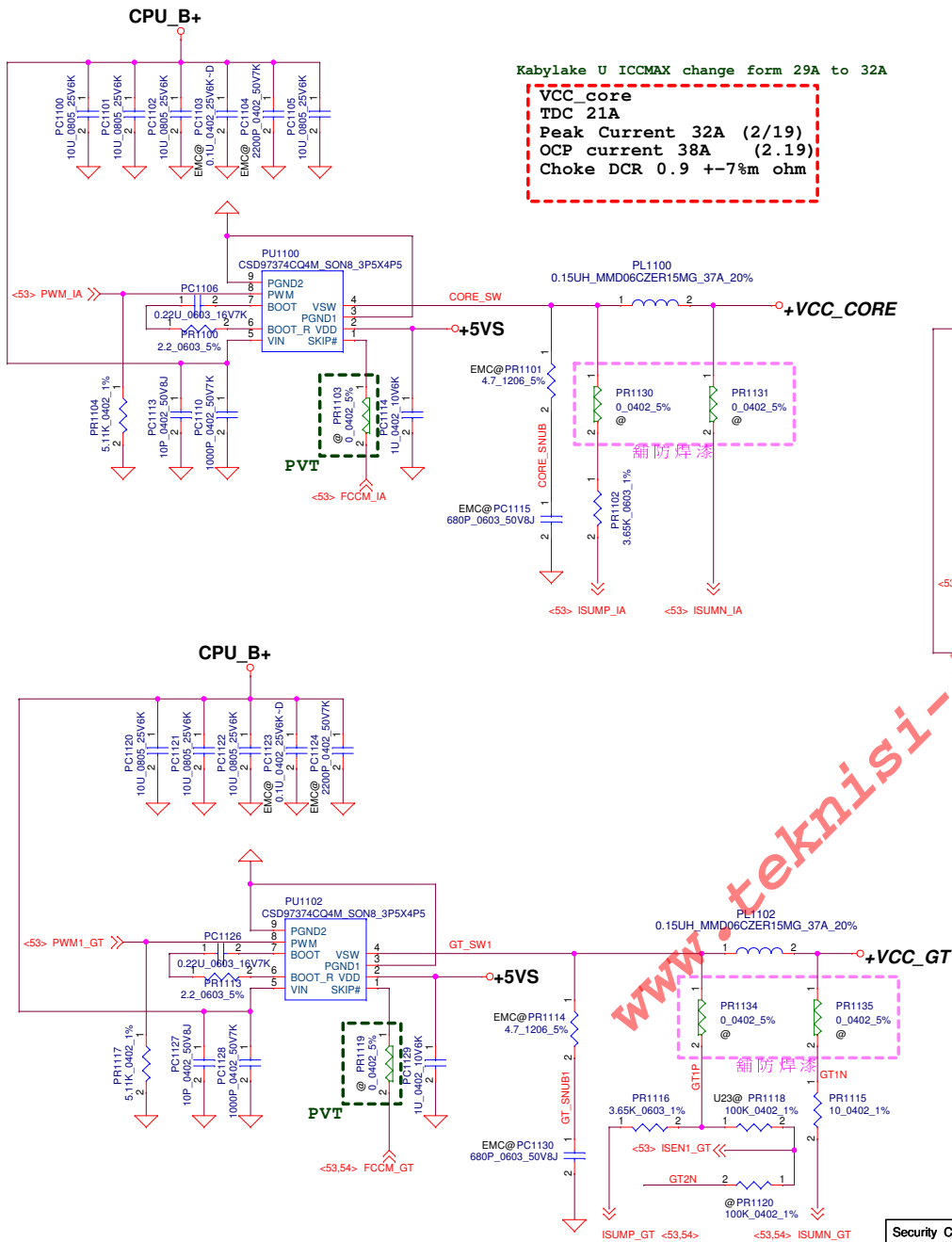
TI FAE Andrew suggest
Cell pin set the voltage of
three cell (13.5V) for OVP

Charger controller(40.1), Support component(40.2)



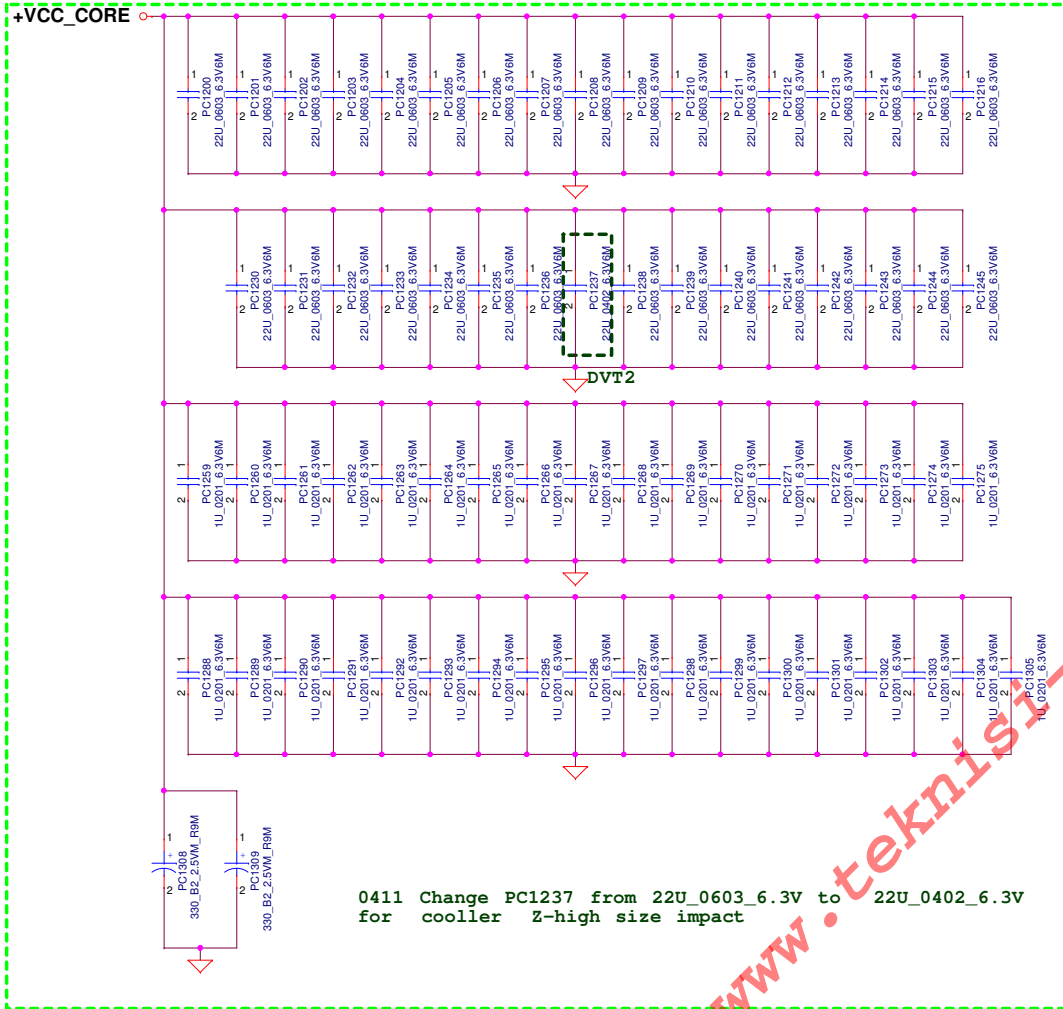
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2014/10/17		Title	
		Deciphered Date		2014/12/05	
				P46-PWR Charger	
				LAD841P	
				Date: Wednesday, August 31, 2016	
				Sheet 46 of 59	





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Size	Document Number	Rev		1.0	
Date:	Wednesday, August 31, 2016	ISheet	54	of	59

VCC_CORE Place on CPU
TOP Side.
22U_0603 * 26 pcs +1U_0201*33 pcs
Bottom Side.
330u_B2*2 pcs + 22U_0603 * 7 pcs + 1U_0201 *2



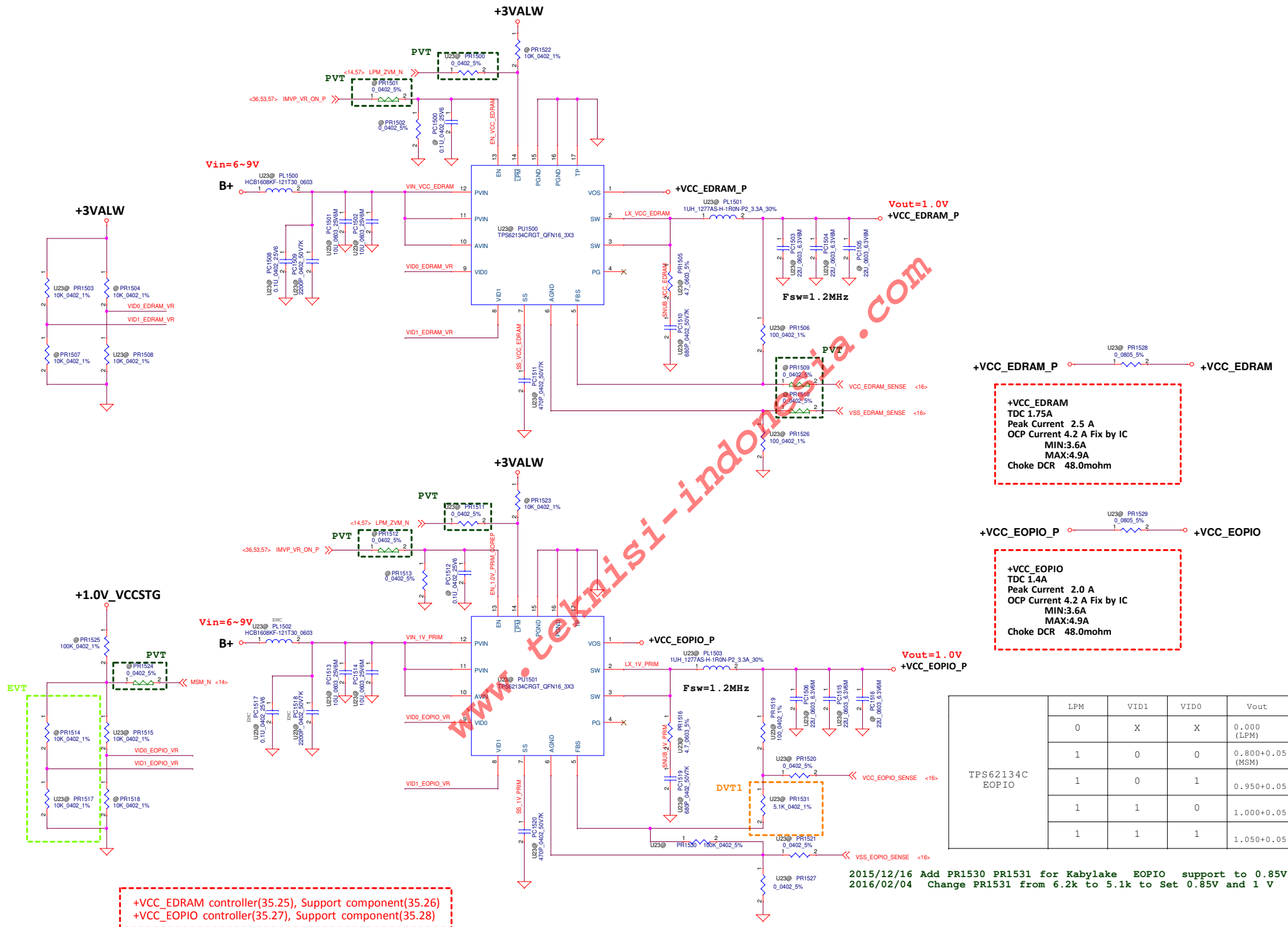
VCC_SA Place on CPU
TOP Side.
22U_0603 * 10 pcs + 1U_0201*7 pcs
Bottom Side.
22U_0603 * 2 pcs

VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

VCC_GT Place on CPU
TOP Side.
22U_0603 * 34 pcs +10U_0603*11 pcs +1U_0201*18 pcs
Bottom Side.
330u_B2*4 pcs



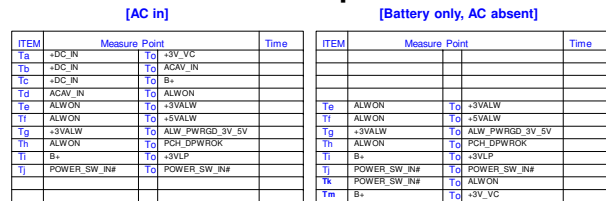
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title		
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				Size		
				Document Number		Rev
				LAD841P		1.0
				Date:		Wednesday, August 31, 2016



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				Size	Document Number	Rev
				LA-C881P		1.0
Date:		Wednesday, August 31, 2016		Sheet	58 of 59	



T10	PCH_RSMRST#	Io	AC_PRESENT	
T11	PCH_RSMRST#	Io	SIO_SLP_S5#	
T12	SIO_SLP_S5#	Io	SIO_SLP_A#	
T13	SIO_SLP_S5#	Io	SIO_SLP_WDAN#	
T14	SIO_SLP_WDAN#	Io	AUX_EN_WOVL	
T15	AUX_EN_WOVL	Io	+3VS_NGFF	
T16	SIO_SLP_S5#	Io	SIO_SLP_S4#	
T17	SIO_SLP_S4#	Io	+1.0V_VCCST	
T18	SIO_SLP_S4#	Io	SUS_ON_EC	
T19	SUS_ON_EC	Io	+1.8VU	
T20	SUS_ON_EC	Io	+1.2V_DDRH	
T21	SIO_SLP_S4#	Io	VCCST_PWROK	
T22	SIO_SLP_S4#	Io	SIO_SLP_S3#	
T23	SIO_SLP_S3#	Io	RUN_ON_EC	
T24	RUN_ON_EC	Io	+3VIOX_SIO	
T25	RUN_ON_EC	Io	+1.6VS_VCCSTG	
T26	RUN_ON_EC	Io	+1.5VS_VCCIO	
T27	RUN_ON_EC	Io	+3VS	
T28	RUN_ON_EC	Io	+3VS	
T29	+3VS	Io	RUNPWROK	
T30	+3VS	Io	MVP_VR_ON	
T31	MVP_VR_ON	Io	VCORE_PG (PCH_PWROK)	
T32	VCORE_PG (PCH_PWROK)	Io	+VCC_SA	
T33	MVP_VR_ON	Io	+VCC_EOPRAM	
T34	MVP_VR_ON	Io	+VCC_EOPIO	
T35	MVP_VR_ON	Io	SYS_PWROK (RESET_OUT#)	
T36	PCH_PLTRST#	Io	+VCC_CORE	
T37	PCH_PLTRST#	Io	+VCC_GT	